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Entitled

Design, Maintenance, Service and Operation EKVM "Soemtron-220"

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It has been published by us to disseminate information about the Soemtron 22x range of electronic desk calculators manufactured by V.E.B. (*1) Büromaschinenwerk Sömmerda, as a project to gather and centralise whatever information can be found about these increasingly rare early electronic calculators.

If you have or know of any information, books, drawings, circuits, hardware, test equipment (prufgerat) or other memorabilia relating to the Soemtron 220, 221, 222 or 224 calculators, their trade names - Daro or Soemtron, manufactured by - V.E.B. Büromaschinenwerk Sömmerda, please email us at - mike@soemtron.org

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With this effort in mind some of the syntax presented here is a little strange to say the least!. Some portions have been reworked to be more readable English text but there is obviously more to be done. If you can help with this, or indeed have any helpful information or comments, please email us at - mike@soemtron.org

Please use, and hopefully enjoy, this in information in the spirit in which we undertook to generate it - as an information source for an interesting piece of early calculator history before the advent of modern electronics, in the days when "hands on" engineers thought through the problems and challenges of designing equipment with little resources, to produce the best end product they could.

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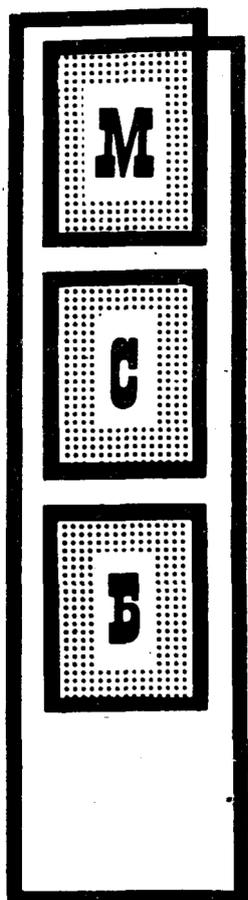***1 - V.E.B - Volkes Eigener Betrieb = Peoples Owned Company**

А. Г. БОБРОВ, И. И. БИГЛЕР

Design, Maintenance Service and Operation EKVM "Soemtron-220"

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The questions of administrative decision of work is at present now inseparably connected with the application of contemporary computer technology, with one of the most of labour-consuming divisions appears the processing of economic information. In recent years fast manufacturing growth and the introduction of a large quantity of electronic key-actuated computers for processing of economic information has been seen. The effective application of new high-productivity electronic key-actuated computers requires the imperative systematic preparation and increasing qualification standard of maintenance of personnel.

This manual is written in strict conformity with the course program of the study of "Soemtron-220" machines in the training network of the main administration of preparation and increase in the qualification of the workers of the calculation of TscSu of the USSR (Central Statistical Office of the USSR). The primary goal of the present manual is to render assistance to the pupil, students of corresponding specialities, and also workers of computing stations and bureau in the application and studying of a design and service maintenance of the electronic keyboard computer "Soemtron-220".

A characteristic property in the construction of the machine is the use of "AND" logic circuits, and the wide application of controlled differentiating circuits, I.E. differentiating circuits with the performance of logical functions.

Chapter I

DESIGN AND THE APPLICATION OF EKVM* "SOEMTRON-220"

1.1.　　　TECHNICAL AND OPERATING CHARACTERISTICS

1.1.1.　　　Purpose and the general description.

The electronic computer model "Soemtron-220" (Fig. 1) can be related to the type of electronic key-actuated computers with manual entry of information with a sequential operating principle. Entry of digital information is provided by the decimal digital keyboard.

The keyboard allows the input of decimal digital information. The arithmetic operations of Addition, Subtraction (balancing), Multiplication, Division and Exponentiation are carried out taking into account the sign of the number. The arithmetic operations of Multiplication and Division are carried out with the set degree of accuracy and with a rounding off of the last digit.

The memory unit consists of three operational and three accumulator registers each with a capacity of 15 digits.

Display of entered information and the results of calculations are provided by 15 digital lamps. The sign of the number is shown by the "─ " sign indicator.

The presence of the accumulator registers ensures appropriate effectiveness during the solution of different kinds of tasks, I.E. it creates an opportunity for entry and use of constants, and allows the accumulation and storage of the necessary intermediate and final results of calculations. Except for performance of arithmetic operations, the machine automatically provides control of exceeding register length.

With a system clock pulse frequency of 25KHz. Addition and Subtraction operations occur in 5ms, whilst Multiplication and Division - on average take 0.5 seconds. Presence of an automatic rounding off of the last entry in Multiplication and Division testifies to the convenience and expediency of the machine for processing in economic information applications. This machine can also be successfully used for different technical-engineering calculations.

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* Note - EKVM = Electronic Key-operated Calculating Machine

The unit type principle of the assembly of separate units is assumed as the basis of construction of the machine. Essentially the computer is an arithmetic-logic unit, whose design is made on the basis of diode-transistor elements in combination with a magnetic storage array composed of ferrite cores, assembled into digital matrices.
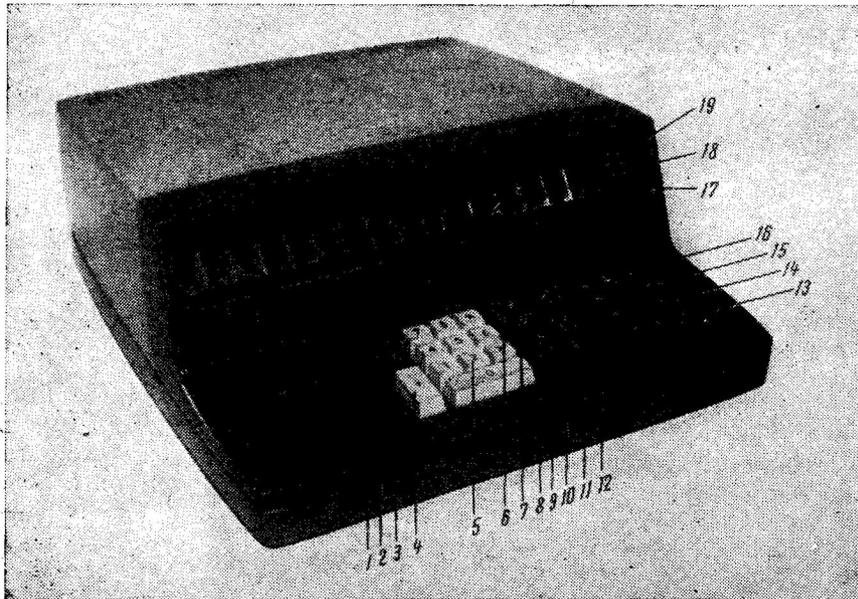

Fig. 1. The common form of electronic key-actuated computer "Soemtron-220":

1 - Rotary decimal point selection switch; 2 – Lö key clears the machine and erases information in the operational registers; 3 - Clear entry key for the most recently input information; 4 - Decimal point key; 5 - Digital keyboard; 6 - Negate entry key; 7 - Multiplication; 8 - Addition, 9 - Involution; 10 - Division; 11 - Subtraction; 12 - Result key; 13 - Add to accumulator registers 1-3; 14 - Subtract from accumulator registers 1-3; 15 - Return the intermediate sum of accumulator registers 1-3; 16 - Return final sum of accumulator registers 1-3; 17 - Digital display; 18 - "—" sign indicator; 19 - Mains on indicator.

The memory unit consists of six independent memory registers MD, MR, AC0, AC1, AC2 and AC3, each of which is capable of storing 15 decimal digits of information plus the sign of the number.

According to its designation the registers can be divided into the operational (MD, MR and AC0) and accumulating (AC1, AC2 and AC3).

The operational registers serve to store the entered digital information, sign of the number and intermediate and final results of the arithmetic operation performed.

The accumulator registers are used for storing of digital information, also the sign of the number, intermediate and final results of calculations.

Digital information, sign of the number, and the arithmetic operation are entered into the arithmetic-logic unit during closing and switching of the corresponding contacts of the digital and functional keys on the keyboard.

The entered digital information, results of arithmetic operations, intermediate and final results of calculations are displayed on the display unit using luminous digital lamps. The display unit has a maximum capacity of 15 decimal digits plus sign.

The integer part of the number is separated from the fractional by setting the decimal point position switch to the desired degree of calculation accuracy. The selected decimal point position is shown by an illuminated incandescent lamp in the appropriate position of the display.

The integral power unit provides all the necessary operational stabilized and non-stabilized supplies.

The supply line voltage with a frequency of 50Hz must be within the limits 220Vac $^{+10\%}_{-15\%}$, − 110Vac $^{+10\%}_{-15\%}$, at a consumed power of 50 W. Overall size of the machine is: width - 380mm, length - 464mm, height - 194mm, weight - is 15 kg.

1.1.2.   Preparation of the machine for operation.

The computer is delivered from the manufacturer set for a mains supply of alternating current with a voltage of 220V at $^{+10\%}_{-15\%}$ with a frequency of 50 Hz.

Before connecting the machine to the mains supply it is necessary to remove upper rear cover and to check that the voltage selector switch of the power unit corresponds to the line voltage of your mains supply.

The setting of the voltage selector switch on the power unit makes it possible to adjust the machine for connection to the AC mains network for voltages of 220V or 127V. After setting the voltage selector switch to the correct line voltage, the removed cover must be replaced.

The assembled machine with mains supply lead should be connected to the mains supply with a master switch. Rotating the "ON-OFF" switch connects the line voltage to the primary winding of transformer and illuminates the "mains on " pilot lamp on the display unit (Fig. 1).

Pressing the "Lö" key ensures the erasure of the information in the operational registers MD, MR, AC0 and resets the component parts to an initial state, enables the power unit and clears the display. On enabling the power unit, the correct voltages which ensure the operation of the arithmetic-logic and display units, are output. As a result of the controlled erasure of the operational registers this ensures all digital lamps of the display unit show the number zero.

Pressing the keys "*I", "*II", "*III" in sequence ensures the erasure of the accumulator registers AC1, AC2, AC3, I.E. The re-writing of digital information from the accumulator registers AC1, AC2, AC3 into the operational register MR (rewritten digital information in the accumulator registers is not retained) the previously written digital information into register MR is erased during the re-writing from the sequential accumulator register. After recall of the last accumulating register digital information in the MR register is erased by pressing the "C" key.

As a result of this serial operation of the enumerated functional keys the arithmetic-logic unit of the machine is completely prepared for completing arithmetic operations.

Rotating the decimal point selection switch sets the correct level of accuracy for calculations.

1.2.   Performance of arithmetic operations.

Entry of the digital information is made through the digital decimal keyboard by a consecutive set of figures, beginning from the high-order digit of the number (Fig. 1). Entry of mixed digital information occurs with inclusion of the "**,**" key after the whole part of a number. When the entered number has no fractional part and also when the fractional part has smaller quantity of decimal figures, than is established by the decimal point switch, entry of extra zeros is not required.

The position of the decimal point switch provides automatic completion of the length of entered numbers, I.E. The automatic Addition of a corresponding quantity zeros after the inclusion of a necessary functional key. After setting the decimal point switch, the position of the decimal point is shown by an illuminated miniature incandescent lamp between the corresponding digital lamps of the digital display to create the illusion of a ",".

1.2.1.   Addition.

Addition operations are performed by the arithmetic-logic unit with the result of the sum in the operational register AC0 or in the accumulating registers AC1, AC2 or AC3.

For performance of operations in a certain sequence the following function keys are used: "+", "=", "+ I", "+ II", "+ III", "▼I", "▼II", "▼III", "*I", "*II", "*III".

Example 1. $a + b = c$ 197 + 454 = 651.

Order of operation	Function key	Display
1. Erase the operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"0"	000000000000000
3. Enter the first term 197	"+"	000000000000197
4. Enter second term 454	"+"	000000000000454
5. Get the result	"="	000000000000651

Example 2. $a + b = c$ 265,12 + 165,437 = 430,557.

Order of operation	Function key	Display
1. Erase the operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"3"	000000000000000
3. Enter the first term 265,12	"+"	000000000265,120
4. Enter second term 165,437	"+"	000000000165,437
5. Get the result	"="	000000000430,557

The position of the decimal point switch is determined by the required degree of accuracy or by the term with the greatest quantity of the numbers after the decimal point.

Addition with a different number of terms is carried out in a similar manner to the examples above. The small difference is to press the Addition "+" key after the entry of each term independent of the number of terms and continue in this way until a final result is obtained by pressing the "=" key.

To display an intermediate sum you should press the "=" key, after which continue with an Addition "+" key in the usual manner to continue the sequence. In the examples above the obtained sum was written into the operational register AC0. The result key ensures the storage of the digital information and sign of the number into register MR with the erasure of information in register AC0. The transfer of the sum into the accumulator registers is produced by pressing the appropriate

keys "+ I", "+ II", "+ III", which ensure the storage of information from register MR into registers AC1, AC2 and AC3 without the erasure of information in the MR register.

An Addition operation with the use of the accumulator registers is examined below.

Example 3.   *a + b = c*   342,35 + 127,23 = 469,58

Order of operation	Function keys	Display
1. Erase the accumulating registers	"∗I" "∗II" "∗III"	
2. Erase the operational registers	"Lö"	000000000000000
3. Set the decimal point switch	"2"	0000000000000,00
4. Enter the first term 342,35	"+ I"	0000000000342,35
5. Enter second term 127,23	"+ I"	0000000000127,23
6. Get the result	"∗I"	0000000000469,58

In this example the obtained sum was written into register AC1. With the serial use of the "+ I ", "+ II", "+ III" keys the sum of 469,58, besides register AC1, will also be written into registers AC2 and AC3. Pressing the "∗1" key ensures the recall of the contents from register AC1 into MR with the erasure of the contents in register AC1.

After completion of the Addition operation with storage of the sum in registers AC1, AC2 and AC3, pressing the corresponding key "+▼I", "+▼II", "+▼III" ensures the display of the intermediate sum, I.E. recall without the erasure from registers AC1, AC2 and AC3 into register MR consequently, after pressing the keys for intermediate sums the information in the appropriate registers remains.

1.2.2.   Subtraction.

A Subtraction operation is carried out by the arithmetic unit with storage of a difference in he operational register AC0 or in accumulating registers AC1, AC2 and AC3.

The display of negative values of the entered digital information is ensured by illumination of the miniature incandescent lamp "─".

For completion of an operation in the specific sequence these functional keys are used:
"+", "- ", "=", "+ I", "+ II", "+ III", "- I", "- II", "- III", "▼I", "▼II", "▼III", "∗I", "∗ II", "∗ III".

Example 4.   *a – b = c*   397,46 – 123,134 = 274,326

Order of operation	Function keys	Display
1. Erase the accumulating registers	"* I" "* II" "* III"	
2. Erase the operational registers	"Lö"	000000000000000
3. Set the decimal point switch	"3"	0000000000000,00
4. Enter minuend 397,46	"+"	0000000000397,460
5. Enter subtrahend 123,134	"─"	0000000000123,134–
6. Get the result	"="	0000000000274,326

The position of the decimal point switch is the same as that used for Addition. Subtraction with a large quantity of subtrahends is carried out in a similar manner to the examples above. The small difference is to press the subtract key "─" after the entry of each subtrahend independent of their quantity and to continue in this way until a final result is obtained by pressing the "=" key.

In this example the difference obtained was written into the operational register AC0. Pressing the result key ensures the return of information from the AC0 register into the MR register with the erasure of the information in the AC0 register.

The transfer of difference into the accumulator registers is produced by pressing "+ I", "+ II", "+ III" keys, which ensure the storage of information from register MR into the appropriate registers AC1, AC2, AC3 without the erasure of information in the MR register.

Below is an example of Subtraction using the accumulator registers.

Example 5.   *a – b = c*   679,38 - 243,15 = 436,23

Order of operation	Function keys	Display
1. Erase the accumulating registers	"* I" "* II" "* III"	
2. Erasure the operational registers	"Lö"	000000000000000
3. Set the decimal point switch	"2"	0000000000000,00
4. Enter minuend 679,38	"+"	0000000000679,38
5. Enter subtrahend 243,15	"- I"	0000000000243,15–
6. Get the result	"*"	0000000000436,23

In the given example the difference obtained was written into register AC1. With serial use of the "+ I", "+ II", "+ III", "- I", "- II", "- III" keys, the Subtraction result 436,23, besides register AC1, will also be stored into registers AC2 and AC3,

Pressing the "* I" key ensures the recall of difference from the AC1 register into the MR register with the erasure of register AC1. After completion of the Subtraction operation with the storage of the difference in registers AC1, AC2 and AC3, pressing the "▼I", "▼II" and "▼III" keys ensures the display of the intermediate difference, I.E. The recall of information without the erasure from the appropriate registers AC1, AC2 or AC3 into the MR register. Consequently, after pressing those keys the information in registers remains.

Example 6. $a - b = - c$ when $a < b$
235,24 - 467,496 = - 232,256 (striking a balance)

Order of operation	Function key	Display
1. Erase the operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"3"	000000000000,000
3. Enter of minuend 35,24	"+"	000000000235,240
4. Enter of subtrahend 467,496	"—"	000000000467,496–
5. Get the result	"="	000000000232,256–

When as a result the completion of any operation gives a negative result, the miniature incandescent lamp is illuminated, to show a display of sign "—".

Example 7.   **(a) + (-b) = - c**
(+ 479,43) + (- 735,64) = - 256,21

Order of operation	Function key	Display
1. Erase the operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"2"	0000000000000,00
3. Enter the first term 479, 43	"+"	0000000000479,43
4. Enter second term 735,64 and press negation "-#" key	"+"	0000000000735,64–
5. Get the result	"="	0000000000256,21–

Example 8.   **(+a) – (–b) = c**
       (+398,49) – (– 635,78) = 1034,27

Order of operation	Function key	Display
1. Erase the operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"2"	0000000000000,00
3. Enter of minuend 398,49	"+"	0000000000398,49
4. Enter subtrahend 635,78 and press negation "-#" key	"—"	0000000000635,78–
5. Get the result	"="	0000000001034,27

Example 9.   **(a+b) – (c+d) + (k–l) = z**
       (235,46 + 1357,28) – (174,27 + 459,96) + (547,54 – 2375,49) = – 869,44

Order of operation	Function key	Display
1. Erase accumulator registers	"* I", "* III", "* III"	
2. Erase the operational registers	"Lö"	000000000000000
3. Set the decimal point switch	"2"	0000000000000,00
4. Enter the first term 235,46	"+ I"	0000000000235,46
5. Enter second term 1357,28	"+ I"	0000000001357,28
6. Result of the first sum	"▼I"	0000000001592,74
7. Enter third term 174,27	"+ II"	0000000000174,27
8. Enter fourth term 459,96	"+ II"	0000000000459,96
9. Result of the second sum	"▼II"	0000000000634,23
10. Subtract second accumulator register from the first	"- I"	0000000000634,23
11. Result of first and second sums	"▼I"	0000000000958,51
12. Enter minuend 547,54	"+ III"	0000000000547,54
13. Enter subtrahend 2375,49	"- III"	0000000002375,49
14. Result of the third sum	"▼III"	0000000001827,95–

Order of operation	Function key	Display
15. Add to third accumulating register	"+ I"	0000000001827,95–
16. Final result	"* I"	0000000000869,44–

Shown below is example 9 using just one of the accumulating registers.

Order of operation	Function key	Display
1. Erase accumulator registers	"* I", "* II", "*III"	
2. Erase the operational registers	"Lö"	000000000000000
3. Set the decimal point switch	"2"	0000000000000,00
4. Enter the first term 235,46	"+"	0000000000235,46
5. Enter second term 1357,28	"+"	0000000001357,28
6. Result of the first sum	"="	0000000001592,74
7. Store in first accumulator register	"+ I"	0000000001592,74
8. Enter third term 174,27	"+"	0000000000174,27
9. Enter fourth term 459,96	"+"	0000000000469,96
10. Result of the second sum	"="	0000000000634,23
11. Subtract second sum from first	"–I"	0000000000634,23
12. Enter minuend 547,54	"+"	0000000000547,54
13. Enter subtrahend 2375,49	"—"	0000000002375,49–
14. Result of the third sum	"="	0000000001827,95–
15. Add the result from the MR register to the first accumulator register	"+ I"	0000000001827,95–
16. Display the final result of the calculation	"+ I"	0000000000869,44–

It is evident from the above examples that algebraic calculation of Addition and Subtraction with sign is accomplished by the arithmetic-logic unit of the machine.

1.2.3.   Multiplication.

Multiplication is carried out by arithmetic-logic unit with the result stored in the operational register MR. To complete the operation in the specific sequence the function keys "X" and "=" are used. The result, found in the operational register MR, can be stored in the three accumulator registers by pressing the function keys "+ I", "+ II", "+ III", "- I", "- II", "- III", a consequence of which adds or subtracts the result to the current information in the accumulator registers.

Completing a Multiplication process automatically rounds off the result at the last step.

Example 10.   **a x b = c**   125,25 x 15,25 = 1910,0625

Order of operation	Function key	Display
1. Erase the operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"4"	00000000000,0000
3. Enter the multiplicand 125,25	"X"	00000000125,2500
4. Enter the multiplier 15,25 and obtain the result	"="	00000001910,0625

Example 11.   **a x b = c**   123,12 x 0,51 = 62,7912

Order of operation	Function key	Display
1. Erase the operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"2"	0000000000000,00
3. Enter the multiplicand 123,12	"X"	0000000000123,12
4. Enter the multiplier ,51 and obtain the result	"="	0000000000062,79

The position of the decimal point switch is determined by the required degree of accuracy of the calculation or by the sum of the number of decimal digits of the factors.

Example 12. **a x b x c = z**   23,5 x 12,5 x 2,12 = 622,75

Order of operation	Function key	Display
1. Erasure of operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"2"	0000000000000,00
3. Enter first factor 23,5	"X"	0000000000023,50
4. Enter second factor 12,5 and obtain the result	"="	0000000000293,75
5. Prepare for multiplication by the third factor	"X"	0000000000293,75
6. Enter the third cofactor 2,12 and obtain the result	"="	0000000000622,75

The operational capabilities of the machine make it possible to perform Multiplication with the use of constants.

An example of Multiplication with a constant coefficient is examined below.

Example 13.   **a x b = c**   125 x 5,3 = 622,5
                     d x b = z   15,36 x 5,3 = 81,408

Order of operation	Function key	Display
1. Erase accumulator registers	"* I", "* II", "* III"	
2. Erase the operational registers	"Lö"	000000000000000
3. Set the decimal point switch	"2"	0000000000000,00
4. Enter constant factor 5,3	"X^N"	0000000000005,30
5. Enter first factor 125,		0000000000012,50
6. Get the result	"X^N"	0000000000622,50
7. Enter second factor 15,36		0000000000015,36
8. Get the result	"X^N"	0000000000081,41

The calculation of sum or difference products is carried out with use of one of the accumulator registers.

Example 14. **(a x b) + (c x d) = z**
     (25 x 10,3) + (17,2 x 5,1) = 345,22

Order of operation	Function key	Display
1. Erase accumulator registers	"* I", "* II", "* III"	
2. Erase the operational registers	"Lö"	000000000000000
3. Set the decimal point switch	"1"	00000000000000,0
4. Enter first factor 25,	"X"	00000000000025,0
5. Enter second factor 12,5 and obtain the result	"="	00000000000257,5
6. Store result in an accumulator register	"+ I"	00000000000257,5
7. Enter third factor 17,2	"X"	00000000000017,2
8. Enter fourth factor 5,1 and obtain the result	"="	00000000000087,7
9. Add first and second products	"+ I"	00000000000087,7
10. Get the result	"* I"	00000000000345,2

The calculation of a difference in two products (a x b) - (c x d) = x, is carried out in a sequence, analogous to the calculation of the sum of two products, with a difference, such that at point 9 of example 14 press the "- I" key instead of the "+ I" key.

In the case of the negative value of cofactors, after the entry of a multiplicand or coefficient the key for the entry of negative values is used. The arithmetic-logic unit of machine accomplishes the operation of Multiplication taking into account the signs of cofactors.

Example 15. **(–a) x (–b) = +c**
     (–24,5) x (–3,75) = 91,875.

Order of operation	Function key	Display
1. Erase the operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"2"	000000000000000

Order of operation	Function key	Display
3. Enter first factor 24,5 Negate value key "-#"	"X"	0000000000024,50 –
4. Enter second factor 3,75 Negate value key "-#"	"—"	0000000000003,75–
5. Get the result	"="	0000000000091,88 –

Operation (a) x (–b) = –c is carried out in a similar manner to that in example 15 and is characterized by the fact that after the entry of the first factor the negate entry key "-#" is not used. The calculation of the signs of cofactors is accomplished by the arithmetic-logic unit of the machine of the operation of algebraic multiplication.

1.2.4.   Exponentiation.

Exponentiation is carried out by the arithmetic-logic unit with storage of the result in the operational register MR. For performance of the operation in the specific sequence the functional keys "X" and "X^n" are provided. The result in register MR can be stored in the accumulating registers AC1 - AC3 by pressing the corresponding "+ I", "+ II", "+ III", "- I", "- III", "- III" keys which will add or subtract the result to the current information in the accumulator registers.

Order of operation	Function key	Display
1. Erasure of operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"0"	000000000000000
3. Entry of the number 25	"X"	000000000000025
4. Result of 25 squared	"X^n"	000000000000625
5. Result of 25 cubed	"X^n"	000000000015625
6. Result of 25 quadrupled	"X^n"	000000000390625

With the erection of the negative number into the degree with the even index the result of calculation is positive. With the erection of the negative number into the degree with the odd index the result of calculation is negative.

1.2.5. Division.

Division is carried out by the arithmetic-logic unit with the result stored in the operational MR register. To complete the operation in the specific sequence the function keys **":"**, **"="** are used. The result, found in the operational register MR, can be stored in the three accumulator registers by pressing the function keys **"+ I"**, **"+ II"**, **"+ III"**, **"- I"**, **"- II"**, **"- III"**, which will add or subtract the result to the current information in the accumulator registers.

In the process of completing a Division operation the quotient is automatically rounded off in the last step.

Example 17. **a : b = c**   625 : 5 = 125

Order of operation	Function key	Display
1. Erasure of operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"0"	000000000000000
3. Enter dividend 625	":"	000000000000625
4. Enter divisor 5 and obtain the result	"="	000000000000125

The operational capabilities of machine make it possible to perform the operation of Division with the use of constants of the dividend and divisor.

Example 18. **d : b = c**   143,15 : 8 = 17,89375
             a : b = z   247,232 : 8 = 30,904

Order of operation	Function key	Display
1. Erase accumulator registers	"* I", "* II", "* III"	
2. Erase the operational registers	"Lö"	000000000000000
3. Set the decimal point switch	"3"	000000000000,000
4. Enter first dividend 143,15	":"	000000000143,150

Order of operation	Function key	Display
5. Enter divisor constant 8,	**"+ I"**	000000000008,000
6. Result of first sum	"="	000000000017,894
8. Enter second dividend 247,232	":"	000000000247,232
9. Return result of the first sum	**"▼I"**	000000000008,000
4. Final result	"="	000000000030,904

The position of the decimal point switch is determined by the required degree of accuracy or by the larger number of decimal points from the numbers entered for Division.

Example 19. **a : d = z** 1235,43 : 26 = 47,5265
a : b = c 1235,43 : 47 = 26,2857

Order of operation	Function key	Display
1. Erase accumulator registers	"* I", "* II", "* III"	
2. Erase the operational registers	"Lö"	000000000000000
3. Set the decimal point switch	"2"	0000000000000,00
4. Enter constant dividend 1235,43	"+ I"	0000000001235,43
5. Prepare for Division	":"	0000000001235,43
6. Enter divisor 26, and obtain the result	"="	0000000000047,52
7. Indication of dividend	"▼I"	0000000001235,43
8. Prepare for Division	":"	0000000001235,43
9. Enter divisor 47, and obtain the result	"="	0000000000026, 29

The calculation of sum or difference of the quotients is carried out with use of one of the accumulator registers.

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Example 20.   **(a : b) – (c : d) = z**
          (5625 : 25) – (1234 : 24) = 173,58.

Order of operation	Function key	Display
1. Erase accumulator registers	"∗ I", "∗ II", "∗ III"	
2. Erase the operational registers	"Lö"	000000000000000
3. Set the decimal point switch	"2"	0000000000000,00
4. Enter first sum dividend 5625,	":"	0000000005625,00
5. Enter divisor 25, and obtain the result	"="	0000000000225,00
6. Store result in accumulator register		0000000000225,00
7. Enter second sum dividend 1234,	":"	0000000001234,00
8. Enter divisor 24, and obtain the result	"="	0000000000051,42
9. Subtract second result the from first	"- I"	0000000000051,42
10. Display the result	"∗ I"	0000000000173,58

   The calculation of the sum of two quotients is carried out in a sequence, analogous to the calculation of a difference of two quotients. The difference is to press the functional key "+ I", instead of "- I" (point 9 of example 20).

   For negative value dividends and divisors press the negate value key "-#" after entering the dividend. Division is carried out taking into account the signs of the dividend and divisor.

Example 21.   **(–a) : (–b) = c** (– 3174,6) : (– 13) = 244,2

Order of operation	Function key	Display
1. Erase the operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"1"	00000000000000,0
3. Enter dividend 3174,6 Negate value key "-#"	":"	0000000003174,6
4. Enter divisor 13, Negate value key "-#"	"+ I"	00000000000013,0–
5 Result	"="	00000000000244,2

The calculation of the signs of the dividend and divisor is accomplished by the arithmetic-logic unit of the machine of the operation of algebraic division.

1.2.6. Extraction of square root.

In normal operation of the computer there is no facility for the automatic extraction of square roots. In this case the most convenient method for the extraction of a square root is to use the sequential approximation method.

For the expression $y_n + 1 = 0.5\left(\dfrac{x}{y_n} + y_n\right)$, where an accurate result is usually found after the third approximation.

Prior to the beginning of calculation the radicand should be broken on the verge of two numbers to the left from the decimal point. The quantity of sides defines quantity of categories of the whole part of a root. In the first approximation, the root is evaluated according to the left face, in which there can be one number.

In the process of calculation to increase the accuracy of the result it is desirable to perform intermediate operations with the largest possible quantity of the decimal digits.

Example 22. $\sqrt{985,96} = 31,4$.

Root from 9 composes 3. Two faces of the integer part of radicand X give the two-digit number of $y_n = 30$.

The result of the first approximation will be:

$$\frac{0,5 \ x \ 985,96}{30} + 30 = 31,432667$$

(Checking: $31,432667^2 = 988,012555$);

The result of the second approximation

$$\frac{0,5 \ x \ 985,96}{31,432667} + 31,432667 = 31,400017$$

(Checking: $31,400017^2 = 985,961068$);

The result of the third approximation

$$\frac{0,5 \ x \ 985,96}{31,400017} + 31,400017 = 31,400000$$

(Checking: $31,4^2 = 985,96$).

Order of operation	Function key	Display
1. Erase accumulator registers	"* I", "* II", "* III"	
2. Erase the operational registers	"Lö"	000000000000000
3. Set the decimal point switch	"6"	000000000,000000
4. Enter dividend 985,96	"+ I"	000000985,960000
5. Prepare for Division	":"	000000985,960000
6. Enter divisor 30,	"+ II"	000000030,000000
7. Result of quotient	"="	000000032,865333
8. Add to accumulator register 2	"+ II"	000000032,865333
9. Get the result	"* I"	000000062,865333
10. Prepare for Division	":"	000000062,865333
11. Enter divisor 2, Result of the first approximation	"="	000000031,432667
12. Store the result into accumulator register	"+ II"	000000031,432667
13. Recall to the operational register and show result of dividend	"▼ I"	000000985,960000
14. Prepare for Division	":"	000000985,960000
15. Recall to the operational register and show result of dividend	"▼ II"	000000031,432667
16. Get the result	"="	000000031,367367
17. Add to accumulator register 2	"+ II"	000000031,367367
18. Get the result	"* II"	000000062,800034
19. Prepare for Division	":"	000000062,800034
20. Enter divisor 2, Result of the first approximation	"="	000000031,400017
21. Add to accumulator register 2	"+ II"	000000031,400017
22. Recall to the operational register and show result of dividend	"▼ I"	000000985,960000
23. Prepare for Division	":"	000000985,960000

Order of operation	Function key	Display
24. Recall accumulator 2, Divide	"▼ II"	000000031,400017
25. Quotient result	"="	000000031,399983
26. Add	"+ II"	000000031,399983
27. Get the result	"* II"	000000062,800000
28. Division	":"	000000062,800000
29. Enter divisor 2, and obtain the result	"="	000000031,400000
30. Result of the third approximation	"X"	000000031,400000
31. Checking	"Xⁿ"	000000985,960000

1.2.7.   Examples of the completion of complex calculations.

Example 23,   **a x (b + c – d) = z**
$$123,15 \; x \; (6,4 + 31 - 0,75) = 4513,4475.$$

Order of operation	Function key	Display
1. Erase the operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"2"	0000000000000,00
3. Enter multiplicand 123,15	"X"	0000000000123,15
4. Enter the first term 6,4	"+"	0000000000006,40
5. Enter second term of 31,	"+"	0000000000031,00
6. Enter subtrahend 75	"-"	0000000000000,75–
7. Get the result	"="	0000000004513,45

Example 24.   **a : (b + c – d) = z**
$$1127: (25,471 + 31,74 - 7,15) = 22 \; 51311$$

Order of operation	Function key	Display
1. Erase the operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"3"	000000000000,000
3. Enter dividend 1127,	":"	000000001127,000

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Continuation

Order of operation	Function key	Display
4. Enter the first term 25,471	"+"	000000000025,471
5. Enter second term 31,74	"+"	000000000031,740
6. Enter subtrahend 7,15	"–"	000000000007,150–
7. Get the result	"="	000000000022,513

Example 25.   **(a x b) : c = z**
     (125 x 25) : 7,3 =428,0821

Order of operation	Function key	Display
1. Erasure of operational registers	"Lö"	000000000000000
2. Set the decimal point switch	"2"	0000000000000,00
3. Enter the first cofactor 125,	"X"	0000000000126,00
4. Enter second cofactor 25,	"="	0000000003125,00
5. Division	":"	0000000003125,00
6. Enter divisor 7,3 and obtain the result	"="	0000000000428,08

Example 26. $\dfrac{a \times b}{c} - \dfrac{d \times l}{y} = z$

$$\frac{135 \times 3,7}{2,4} - \frac{35 \times 27,3}{12} = 128,50$$

Order of operation	Function key	Display
1. Erasure of accumulator registers	"* I", "* II", "* III"	
2. Erasure of operational registers	"Lö"	000000000000000
3. Set the decimal point switch	"2"	0000000000000,00
4. Enter cofactor 135,23	"="	0000000003125,00

Order of operation	Function key	Display
5. Enter cofactor 3,7 and obtain the result	"="	0000000000499,50
6. Divide	":"	0000000000499,50
7. Enter divisor 2,4 and obtain the result	"="	0000000000208,13
8. Store quotient to accumulator 1	"+ I"	0000000000208,13
9. Enter cofactor 35,	"X"	0000000000035,00
10. Enter cofactor 27,3 and obtain the result	"="	0000000000955,50
11. Division	":"	0000000000955,50
12. Enter divisor 12, and obtain the result	"="	0000000000079,63
13. Subtract	"– I"	0000000000079,63
14. Calculation result	"* I"	0000000000128,50

The calculation of $\dfrac{a \times b}{c} = \dfrac{d \times l}{y} = z$ is carried out in the sequence of the given example above but is characterized by the fact that at point 13 instead of using the Subtraction from accumulator key "- I", the Add to accumulator key "+ I" is used.

Chapter II

**ELEMENTS of pulse TECHNIQUE
AND POWER SUPPLY**

II. 1.   BLOCK DIAGRAM OF THE MACHINE.

All necessary information enters the arithmetical and storage unit by pressing the appropriate keyboard digital and functional keys in a specific sequence (Fig. 2).

The entry of digital information for the completion of arithmetic operations and different calculations is ensured by the decimal digital keyboard.

The encoding of the input information encodes the inputted digital information from the keyboard from the decimal system into the Binary Coded Decimal numeration system.

The coded digital information from the encoder output is in proportion to the collection.

The entered number is passed to the arithmetic-logic unit and is stored in the appropriate part of the ferrite core memory in the operational register MR.

The management teams and arithmetic operations are carried out the functional keys for input unit. Pressing one of the functional keys causes the completion of the corresponding operation in the arithmetic-logic unit.

Fig. 2. Block diagram of a « Soemtron-220 » computer.

All operations in the machine are stored in the ferrite core memory as digital information and are performed in the Binary Coded Decimal numeration system.

The information, written into the four core planes of the MR register by the decoder of arithmetic-logic unit, is transferred from the binary coded decimal numeration system into decimal, the decoded digital information from the output of the decoders is shown by the luminous digital lamps of display unit, which ensures the visual output of the entered information, results of arithmetic operations and different calculations in the decimal system. For visual output of the digital information of the accumulator registers, the appropriate functional keys are used, which ensure the transfer of the digital information in the accumulating register into the operational register MR.

II.2.   ARITHMETIC-LOGIC UNIT

The arithmetic-logic unit consists of 12 boards of printed circuit assemblies with the components of the required electronic circuits, which accomplish different arithmetic operations and calculations.

The diagrams used show the logic functions, switching, memory and amplifier elements of the overall diagram of the arithmetic-logic unit of the computer. Signals formed at the outputs, and also those entering the inputs of the corresponding electronic circuits must be within the limits from 0V to -12V. With the exception of the signals, which are formed by the anode and cathode amplifier circuits for the display.

It is customary that those signals entering the inputs or formed at outputs of the corresponding electronic circuits, in the voltage range from 0V to -1,5V are assumed to be a logic 0 signal. Voltages in the range from -8V to -12V are assumed to be a logic 1 signal.

The arithmetic-logic unit through appropriate connectors is connected to the power unit, input unit, display unit and decimal point position switch circuits to make the overall electrical diagram of machine.

On the basis of a number of the design features of the machine, the memory unit is considered as a separate unit in the composition of the arithmetic-logic unit.

Note. In the schematic circuits, transistor part numbers indicated in brackets were those established and used in the appropriate schematics of the units and components of the first release machines.

11.3.   ELEMENTS OF THE FUNCTIONAL DIAGRAM.

11.3.1.   AND gate (conjunction).

The diagram shows the logical function "AND", on conditions of which the logic 1 signal at output A of diagram is generated only when all inputs E enter logic 1 level signals. The correct realization of the logical function can only be executed when in the absence of logic 1 signals the appropriate inputs E of the gate enter logic 0 signals.

The diagram is drawn with semiconductor diodes and has one output and can have from 2 to 20 inputs.

On the overall functional diagram of the machine "AND" gates are given numbers from K1 to K211.

The logic symbol and schematic circuit diagram are given in Fig. 3.

An "AND" gate depending on signals at the inputs to E1 - E20 is in the disabled or enabled state.

With all signals at logic 0 on the inputs E1 - E20 of an "AND" gate the diodes are forward biased or turned on resulting in a small forward voltage drop. Current in the circuit: 0V, parallel diodes D1 - D20, resistor R1, -12V - on the small resistance of the forward biased diodes creates an insignificant voltage drop. In essence a voltage drop occurs on the 10 kilohms resistor, therefore, at output A logic 0 signal is generated, which determines the conducting state of "AND" gate.

With simultaneous logic 1 signals to the inputs of E1 - E20 the gate is opened, as a result at the "AND" output a logic 1 level signal is produced.

When one or several inputs E of the gate input signals, the diodes of the corresponding inputs are connected to inverse voltages, I.E. The diodes are forward biased by a logic 0 signal, from the output of one or several forward biased diodes, which ensure the conducting state of the circuit.

Simultaneously input all inputs diagrams logic 0 signals or 1 because of the fluctuations of signal amplitude from 0V to -1,5V and from -8V to -12V are not usually opened and they do not reverse bias all diodes.

At the output of the on or off circuit a logic 0 or 1 signal is generated of a smaller amplitude to all the input signals,

Fig. 3. Logic symbol and circuit diagram of an « AND » gate.

Network elements: resistor R1 = 10 Kilohms; 0,05W; 10%; diodes D1..D20 = 1N35 or GAZ17

which reverse biases all the remaining diodes. Signals with the smaller amplitude provides the conducting state of the corresponding diode and the current in the circuit of diagram, proportional to a potential difference of the input signal and source -12V. The completion of the assigned logical functions by an "AND" gate is ensured only when in the absence of logic 1 signals at the appropriate E inputs a logic 0 signal is input.

When the resistor of an "AND" gate instead of being connected to the power supply -12V is connected to the output of an inverter (I.E. flip-flop, the diagram of joining), the "AND" gate becomes dependent on the signal at output of an inverter, I.E. controlled by the signal from the output of an equivalent component. Consequently the resistor of the circuit diagram becomes a control input.
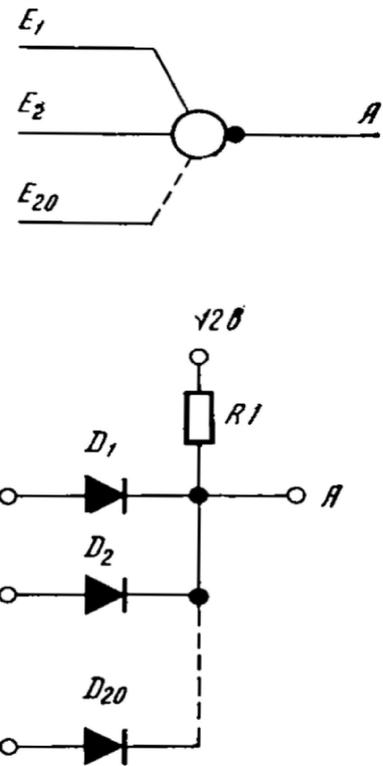
The input of a logic 0 signal at this input blocks the function of the circuit. Input of a logic 1 signal at this input of the "AND" gate does not change the assigned logical functions. This practical control input can be considered as an additional input of an "AND" gate.

II.3.2.   OR gate (disjunction).

The diagram shows the logical function "OR ", on conditions of which a logic 1 signal at output A is generated when one or several inputs E enters a logic 1 signal.
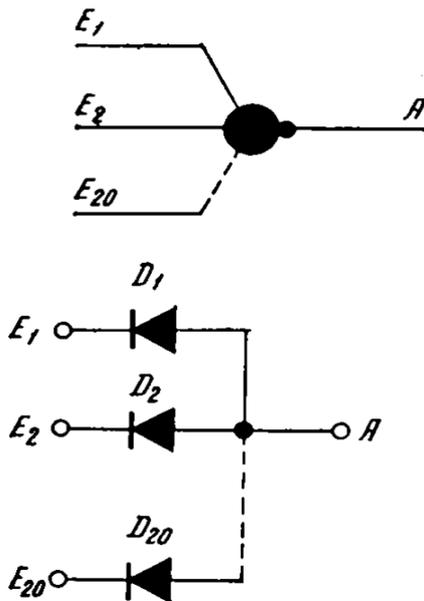

The circuit is drawn with semiconductor diodes and has one output and can have from 2 to 20 inputs. The quantity of diodes in the diagram is determined by the quantity of inputs. The anodes of the diodes are connected to a common point and is the output of the circuit.

In the overall functional diagram of the machine "OR " gates are given gate numbers from D1 to D26. The logic symbol and schematic circuit diagram are given in Fig. 4.

The completion of logical functions by an "OR " gate does not require special circuit conditions, I.E. The connection of logic 0 signals or the presence or absence of logic 1 signals at the inputs of E1 - E20 of the gate. In a number of cases the inputs E of the gate a logic 0 signal is not input.

Fig. 4. Logic symbol and circuit diagram of an « OR » gate.

Network elements: Diodes D1 .. D20 - 1N35 or GAZ17.

When one or several inputs simultaneously input logic 1 signals, the corresponding diodes are forward biased, as a result of which a logic 1 signal is output at point A of the gate. With the larger amplitude of all input signals, which reverse biases the remaining diodes of the gate. In most cases the small resistance of the forward biased diode does not need to be considered.

II.3.3.   Inverter.

The diagram of an inverter shows the logical function "NOT " (negation), the conditions of which a logic 1 signal at output A is only output when input E of the circuit diagram inputs a logic 0 signal, correspondingly, when input E of the circuit is a logic 1 signal, output A of the inverter produces a logic 0 signal.

The circuit of an inverter is executed with a P-N-P type transistor and is a one-stage amplifier.

The logic symbol and schematic circuit diagram of an inverter are given in Fig. 5, on which the dotted line shows the connection point for the source of signals. Let us assume that in the initial state of the inverter diagram a logic 0 signal is applied at input E.
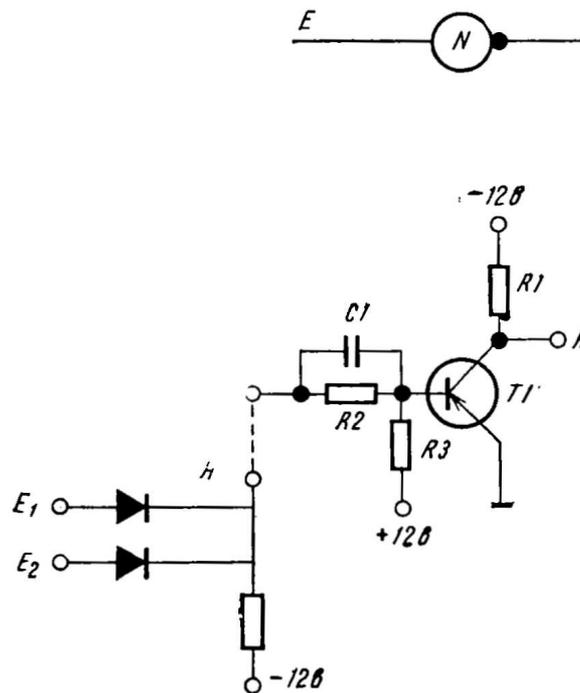

Fig 5. Logic symbol, and circuit diagram of an "Inverter".
Component parts:

Circuit diagram number	Transistor T1	Capacitor C1	Resistor R1	Resistor R2	Resistor R3
Nº 630	SA25/2 (2SB75) $\beta = 29\text{-}55$	1000pF 10% 63V	1K5 10% 0.125W	12K 10% 0.05W	68K 10% 0.05W
Nº 631	SA25/3 (2SB77) $\beta = 45\text{-}88$	1000pF 10% 63V	1K5 10% 0.125W	12K 10% 0.05W	68K 10% 0.05W
Nº 632	SA25/4 (2SB77) $\beta = 72\text{-}166$	1000pF 10% 63V	1K5 10% 0.125W	12K 10% 0.05W	68K 10% 0.05W
Nº 635	SA25/4 (2SB77) $\beta = 72\text{-}166$	1000pF 10% 63V	-	12K 10% 0.05W	68K 10% 0.05W
Nº 636	SA25/3 (2SB77) $\beta = 45\text{-}88$	2700pF 10% 63V	-	4K7 10% 0.05W	39K 10% 0.05W
Nº 637	SA25/4 (2SB77) $\beta = 72\text{-}166$	1000pF 10% 63V	1K5 10% 0.125W	4K7 10% 0.05W	22K 10% 0.05W
Nº 649	SA25/4 (2SB77) $\beta = 72\text{-}166$	220pF 10% 63V	1K5 10% 0.125W	12K 10% 0.05W	68K 10% 0.05W
Nº 651	SA25/2 (2SB75) $\beta = 29\text{-}55$	220pF 10% 63V	1K 10% 0.125W	12K 10% 0.05W	68K 10% 0.05W
Nº 652	SA25/4 (2SB77) $\beta = 72\text{-}166$	470pF 10% 63V	1K5 10% 0.125W	8K2 10% 0.05W	47K 10% 0.05W

The source current flows in the circuit: +12V, resistors R3, R2, 0V into a logic 0 signal of the applied signals. The current is limited by the resistance of the voltage divider resistors.

A voltage drop across resistor R2 from the current of the input bias source creates on the transistor base a positive potential in relation to the emitter, the inverse voltage, applied to the emitter junction, is within the limits of +2V and ensures the non-conducting state of transistor T1. In the base collector chain of the non-conducting transistor flows a current Iko, which creates a small voltage drop across the collector resistor R1. As a result of the non-conducting state of transistor at output A of the inverter a logic 1 is output, until the circuit input E receives a logic 0.

With the connection of a logic 1 signal to input E of the inverter circuit the initial state of C1 shunts the base resistor R2. The negative voltage input logic 1 signal inputs the base and transistor T1 is non-conducting.

In the circuit of the conducting transistor from 0V, T1, R1, -12V flows a collector current, whose value in essence is limited by the resistance of resistor R1.

On the resistance of the conducting transistor thus the current of collector occurs a comparatively small voltage drop. The collector potential becomes close to the emitter potential and so a logic 0 signal is output at point A of the inverter.

Consequently, until input E of the inverter circuit receives a logic 1 signal, output A of the circuit diagram will remain at a logic 0 level.

Capacitor C1 is charged up to the logic 1 signal voltage, the reactance Xc of speed up capacitor C1 increases, to the base current circuit is connected resistor R2, which decreases the value of current, flowing in the circuit: 0V, base-emitter of the conducting transistor, resistor R2 in parallel C1, internal is the resistance of the source of signals, -12V. The voltage between the base and the emitter decreases. The base becomes more positive, but preserves negative potential with respect to the emitter. Transistor T1 remains in the conducting state. The value of the base current from the signal source in essence will be determined by the amplitude of the input signal, by the internal resistance of the signal source and by the resistance of the base resistor R2.

The source current of the displacement flows in the circuit: +12V, resistor R3, resistance of the base-emitter of conducting transistor, 0v. The resistance of R3 considerably exceeds the value of the resistance of the base-emitter of the conducting transistor. The source current of the displacement, in essence, is determined by the resistance of resistor. R3.

The resistance of resistor R3 is approximately 5-7 times the value of the resistance of the base resistor R2. Consequently, the source current of the displacement will be considerably less than the value of the base current. The counter direction of flow of base and source of displacement creates the resulting current in the section of the chain: 0V, the base-emitter of the conducting transistor. The resulting current creates a voltage drop across resistance the base-emitter of the conducting transistor and ensures the negative potential of the base with respect to the emitter, which retains transistor T1 in the conducting state. The conducting transistor can be characterized by the saturated and unsaturated states and the dependence of the relationship of the currents, flowing in the base and collector chains.

If the input current, multiplied by the mu-factor of transistor, is more than the collector current value of βIb that transistor is in the saturated state. If the collector and base current values do not satisfy this relationship, then transistor is in the unsaturated state. The relationship of the current values in the circuit diagram of inverter N630 determines the saturated operating condition of transistor T1. After the end of the logic 1 signal the input of the inverter diagram receives a logic 0 signal.

At the initial moment C1 speed up capacitor shunts the resistor of R2. The base obtains a positive potential with respect to the emitter. Transistor T1 is non-conducting, and output A of the inverter will generate a logic 1 signal. Capacitor C1 is recharged to the value of a voltage drop across resistor R2 from the source current of displacement, the reactance of Xc, increases, to the current circuit of the source of displacement is connected the resistor of R2. A voltage drop across resistor R2 from the current of the source of displacement ensures the non-conducting state of transistor T1.

With the series connection of two inverters the phase of the input signal to input A of the first inverter does not change at output E of the second inverter.

11.3.4.   Driver amplifier.

A driver amplifier (V567 circuit diagram) is the two-stage amplifier, assembled from series-connected inverters. In the second inverter a more powerful transistor is used.

Logic symbol and schematic circuit diagram of the amplifier are given in Fig. 6.

In the initial state input E of amplifier circuit receives a logic 0 signal. The current of the source of displacement flows in the circuit: +12V, R5, R4, 0V and the source of signals. The voltage divider formed from resistors R5, R4 creates on transistor base a positive potential with respect to the emitter and ensures the non-conducting state of transistor T1. Simultaneously the displacement source current flows in the circuit: +12V, resistors R6, R3, R1, -12V. The voltage divider formed from the resistors R1, R3 and R6 creates on the base of transistor T2 a negative potential with respect to the emitter. The forward voltage, applied to the emitter junction, ensures the conducting state of transistor T2.

In the circuits: a) 0V, T2, R3, R1, -12V; and b) +12V, R6, T2, 0V in the conducting transistor flow the base currents and source of the displacement, which have a different value and direction. As a result on the base of transistor T2 remains the negative potential with respect to the emitter, which ensures the conducting state of transistor T2. The current value, flowing in the circuit 0V, T2, R2, -12V, is limited by the small resistance of the conducting transistor T2 and by resistor R2. In the circuit of the conducting transistor T2 a voltage drop in essence it occurs on the collector resistor R2.

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Consequently, until input E of the amplifier receives a logic 0 signal, transistor T2 it is in the conducting state, and output A of the amplifier is at a logic 0 level.

When input E of the amplifier receives a logic 1 signal, at the initial moment capacitor C1's capacity shunts the base resistor R4. The negative voltage of the input signal enters the base of transistor T1.
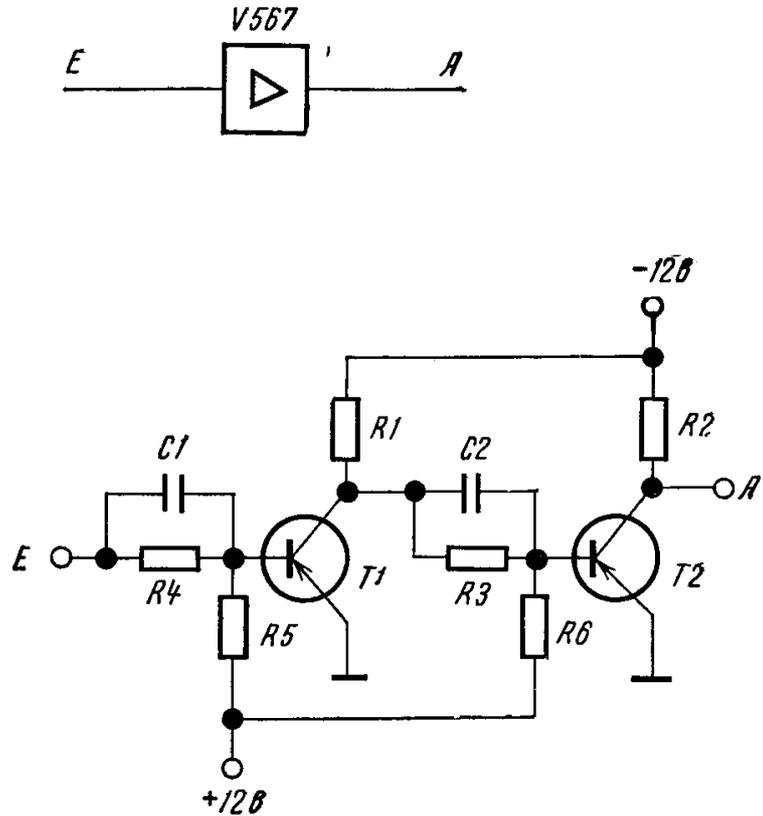

Fig. 6. Logic symbol and circuit diagram of a "Driver amplifier".
Component parts of V567

Transistor T1	SA25/4 (2SB77)	β=72–166
" T2	SA25/4 (2SB77)	β=72–166
Capacitor C1	1000pF 10% 63V	
" C2	2200pF 10% 63V	
Resistor R1	820R 0.25W 10%	
" R2	330R 0.5W 10%	
" R3	2K2 0.05W 10%	
" R4	12K 0.05W 10%	
" R5	68K 0.05W 10%	
" R6	15K 0.05W 10%	

Transistor T1 is conducting and a current is created in the collector circuit: 0V, T1, R1, -12V of the power supply. The value of the collector current is limited by the small resistance of the conducting transistor and by resistor R1. As a result the collector of the conducting transistor T1 generates a logic 0 signal. Capacitor C1 is charged, it's reactance X, increases, to the current circuit of the base is connected resistor R4, which decreases the value of current in the circuit: 0V in, the base-emitter of the conducting transistor T1, R4, and the internal resistance of the source signals -12V.

The voltage between the emitter and the base decreases, so the base becomes more positive, but preserves negative potential with respect to the emitter. Transistor T1 remains in the conducting state.

From the collector of transistor T1 a logic 0 signal enters capacitor C2 and the base resistor R3. At the initial moment the capacitor shunts resistor R3. Positive voltage drop enters the base of transistor T2. The base of transistor obtains a positive potential with respect to the emitter. Transistor T2 is non-conducting.

Capacitor C2 is discharged, the reactance of X, increases, to the chain of the source of displacement is connected resistor R3, which decreases the value of current, flowing in the circuit: +12V, R6, R3, T1, 0v, base becomes more negative, but preserves positive potential with respect to the emitter. Consequently, until input E of amplifier receives a logic 1 signal, transistor T2 is in the non-conducting state, at output A of amplifier it is generated the signal E. After the end of the logic 1 signal the input A of amplifier enters a logic 0 signal. Amplifier circuit returns to the initial state. In this case the speed-up capacitors complete the inverter functions. The capacitor C1 decreases the transit time of transistor T1 into the non-conducting state, while the capacitor C2 decreases the transit time of transistor T2 into the conducting state.

As a result the reverse switching of transistors in accordance with the initial state at output A of amplifier circuit a logic 0 signal is generated.

II.3.5.   Read amplifier.

The read amplifiers (diagram V507/1) serve to read the written information from the ferrite cores of the memory block into the four flip-flops of register A.

Readout is produced from pulses induced by a reversal of the magnetization of the ferrite cores, which directs an EMF onto the read wire.

In turn the read wire is connected to the inputs E2 and E3 of the read amplifier. Taking into account that the reversal of polarity of ferrite cores occurs also during the record of information, the starting of the read amplifier occurs only when its input E1 receives the special reading signal (HV=1). As a result of the special arrangement and routing of cores in the matrix by the read wire can arise both positive and negative polarity pulses, which in equal measure must act on the amplifier in order to obtain a positive polarity pulse at its output.

A logic symbol and schematic circuit diagram of a read amplifier are given in Fig. 7. In the initial state of the amplifier diagram input E1 receives a logic 0 signal, the current of the source of displacement flows in the circuit: +12V, R3, R2, 0V. A voltage divider formed from resistors R2 and R3 creates a positive potential on the base of transistor T1 with respect to the emitter.

Transistor T1 is in the non-conducting state, at output A of the read amplifier circuit is produced a logic 1 signal.

Simultaneously the current of the source of displacement flows in the circuit: +12V, R4, R5, 0V. The voltage divider formed from resistors R4, R5 through the secondary winding of the transformer creates on the bases of transistors T2 and T3 of all four read amplifiers a positive potential, which ensures the non-conducting state of transistors T2 and T3.
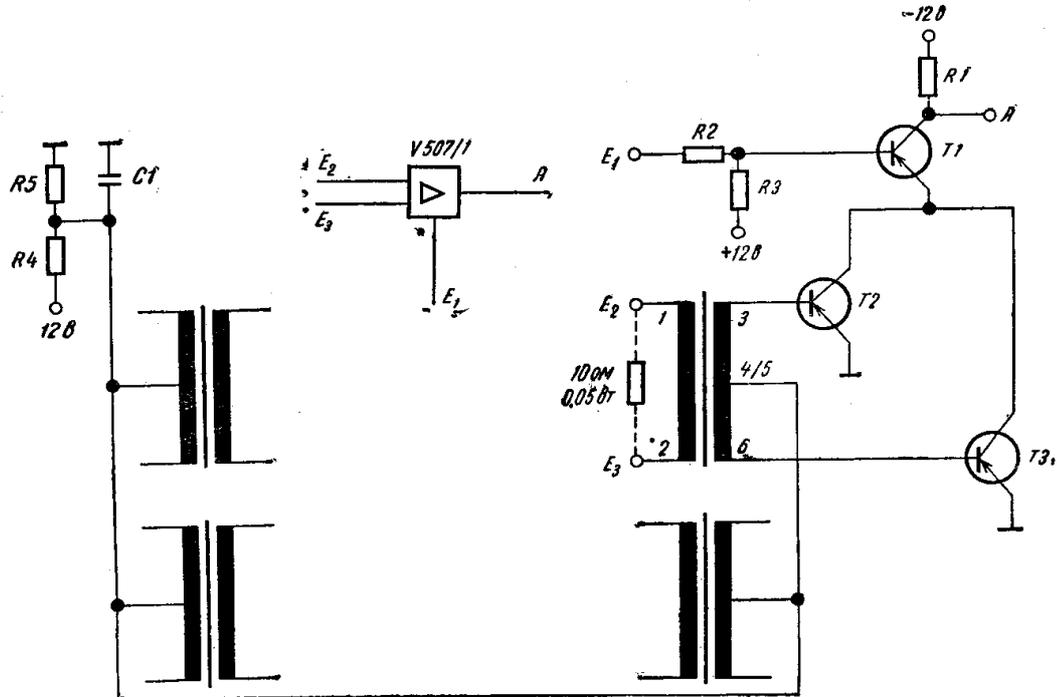

Fig. 7. Logic symbol and circuit diagram of a "Read Amplifier".

Component parts of V507/1:

Transistor T1	SB20/2 (2SA15)	β=29–55
" T2	SB20/3 (2SA15)	β=45–88
" T3	SB20/3 (2SA15)	β=45–88
Capacitor C1	0.047uF 10% 63V	
Resistor R1	10K 0.125W 10%	
" R2	12K 0.125W 10%	
" R3	68K 0.125W 10%	
" R4	6K8 0.125W 5%	
" R5	100R 0.125W 5%	

The operation of the amplifier in shaping the positive polarity pulse at output A of the circuit diagram occurs in the following order. First input E1 receives the drive signal HV=1 and the voltage divider formed from resistors R2 and R3 creates a negative potential on the base with respect to the emitter of transistor T1.

Transistor T1 is conducting and connects the collectors of transistors T2 and T3 to the negative voltage of the power supply -12V.

The emitter of the conducting transistor T1 is connected to 0V through the high resistance of the non-conducting transistors T2 and T3. Consequently, current in the circuit of the conducting transistor T1 increases insignificantly, and the corresponding change in the voltage on output A can be practically ignored.

The polarity reversal of a ferrite core induces an EMF in the region of 30mV on the read wire, which is fed to inputs E2 and E3 of the primary winding of the step-up transformer which has a relationship of 1:100. Let us assume input E2 receives a positive potential from the read wire, therefore, through the primary winding of the transformer from input E2 to input E3 flows a current. An EMF is induced in the secondary winding. The start of secondary winding ensures that the resultant EMF is in the same direction as in the primary winding of transformer.

The positive potential at output 3 of the transformer secondary winding enters the base and does not change the non-conducting state of transistor T2.

The negative potential at output 6 of the transformer secondary windings enters the base and opens transistor T3. At output A of the amplifier a logic signal which changes from 1 to 0.

In the circuit of the conducting transistors 0V, T3, T1, R1, -12V the current value in essence is limited by resistor R1. On the resistances of the conducting transistors T3 and T1 there occurs a comparatively small voltage drop. Transistor T3 is non-conducting after the end of signal at the inputs E2 and E3 of the primary winding of the transformer. The emitter of the conducting transistor T1 is connected to 0V through the high resistance of the non-conducting transistors T2 and T3. Current in the circuit of the conducting transistor T1 sharply decreases, at output of the amplifier occurs a change in the signal from logic 0 to 1. Transistor T1 will be non-conducting after the end of signal E at output E1. If input E2 receives a negative potential from the read wire, instead of transistor T3, transistor T2 will be conducting. As a result output A of the read amplifier generates a positive polarity pulse.

1I.3.6.   RC differentiating circuit.

The most common device for the shaping of peak pulses of differing polarity is the capacitive differentiating circuit RC, which consists of a capacitor C1, resistor R1 and diode D1.

The logic symbol and schematic circuit diagram are given in Fig. 8. Depending on the input connection at E2 the operation of the differentiating circuit occurs with or without logical functions. The connection of input E2 of the differentiating circuit to 0V ensures the circuit operates without logical functions. For with logical functions the differentiating circuit is connected via input E2 to the output of a logical element.

2*

1. Differentiating chain operation without logical functions.

Let us assume that capacitor C1 it is completely discharged, input E1 of the differentiating circuit receives a negative polarity square pulse and so creates a charging circuit for capacitor C1. The voltage across capacitor cannot abruptly change. A current begins to flow in the capacitor charging circuit, whose value is limited by the resistance of resistor R1. At the initial moment the current has a maximum value and diminishes in proportion to the charge of the capacitor.
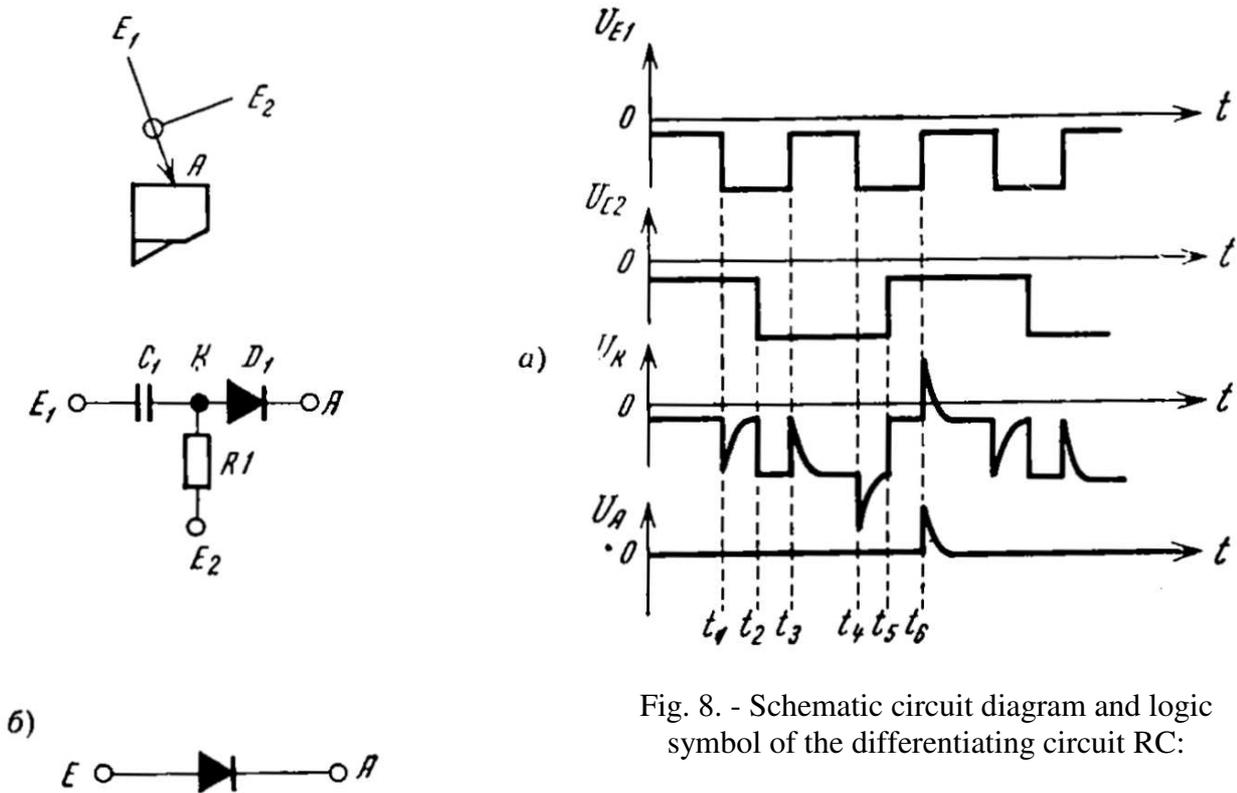
Fig. 8. - Schematic circuit diagram and logic symbol of the differentiating circuit RC:

Diode D1 - 1N35 or GAZ17; Capacitor C1 – 560pF 5% 63V; Resistor R1-10k 0,05 W 10%; A) - diagram of the formation of signals by the differentiating circuit with a control input; B) the diode of the collector input of the flip-flop of 1N35 or GAZ17.

Accordingly at the initial moment of time on resistor R1 occurs the greatest voltage drop, which decreases in proportion to a change in the value of the charge current. As a result diode D1 provides a pulse of negative polarity. After capacitor C1 charges to the voltage of the signal source, current in the differentiating circuit will fall to zero, so the voltage drop across resistor R1 ceases.

The diode D1 enters a voltage, equal to 0V. After the end of the pulse on the differentiating circuit input, a logic 0 signal is input, which corresponds to closing the circuit of the capacitor discharge through resistor R1 without taking into account the small internal resistance of the signal source. Capacitor discharge current flows in the opposite direction. Again at the initial moment the current has maximum value and diminishes in proportion to the capacitor discharge. Accordingly the greatest voltage drop occurs on resistor R1 at the initial moment, which decreases proportionally in response to a change in the value of current over time. As a result of this the diode D1 enters the peak positive polarity pulse.

The described mode of operation of the differentiating circuit occurs with the condition of a large pulse duration at input E1, which enables the capacitor to charge to the voltage of the input signal. It is necessary to keep in mind, that at any moment of time the voltage across capacitor C1 and voltage drop across resistor R1 is equal to the voltage of the source of signal $Vc + Vr = V$. In the machine schematics the differentiating circuit RC is adapted for switching the circuits of a monostable and flip-flops, which are calculated starting from the positive polarity pulses. For this purpose at the output of the chain D1 is connected, which passes positive polarity pulses at output A only and ensures the removal of the negative polarity pulses.

Let us examine the influence of the parameters of the elements of the differentiating circuit on the decrease in the voltage of a peak pulse.

Let us assume that with the given resistance value of resistor R1 with an increased value in the capacitance of capacitor C1, at the initial moment current in the circuit is limited by the constant resistance value of resistor R1 and diminishes in proportion to capacitor charge or discharge. Voltage on resistor R1 relative to 0V of input E2 will fall more slowly, since for discharge or charge of an increased capacitor value by the given current requires a longer time, in consequence of which the duration of the pulse increases. A decrease of the capacitance value causes a more rapid decrease in the voltage on resistor R1, causing the duration of the pulse to decrease. Similarly with a given capacitance value, an increasing or decreasing change in the resistor value leads to the same result. In the first case the voltage on resistor R1 will diminish more slowly than in the second, on the basis of the fact that for the charge on the capacitor value the smaller current requires a greater time n, on the contrary, with a current of larger value - shorter time. The decrease in the voltage on resistor R1 is determined by the time constant of the differentiation chain since, which has a dimensionality of time and most conveniently is determined from the following relationships:

Ohms	x	farads	=	seconds;
Kohms	x	microfarads	=	milliseconds;
Megohms	x	picofarads	=	microseconds

Physically the time constant t can be represented as the time, for which voltage across capacitor changes to 63%, and the value of capacitor charge or discharge current decreases to 37% from the initial value. Let us assume the negative clock pulse of the multivibrator has a duration, equal to 20uS, which let us accept as the minimum at the input of the differentiating circuit. The value of capacitor C1 = 560pF, the resistance of resistor R1 = 10K, the time constant $T = RC$ of the chain will be equal to:

$$0,01 \text{ Megohm x } 560pf = 5,6mS.$$

In practice it is customary to assume the capacitor is charged in a time, equal to 3-5t, which equates to 16,8 - 28,0uS.

In this case the chain's time constant t is equal to approximately 4t, which corresponds to the previously described mode of operation of the differentiating circuit. The differentiating circuit for starting the monostable has a resistor, equal to 4,7 kilohms, and so respectively a smaller value of t and a smaller pulse duration at output.

2.   Differentiating circuit operation with logical functions.

The differentiating circuit diagram forms the logical function "AND", the conditions of which dictate the positive polarity pulse at output A is shaped with the change at input E1 of a logic 1 to 0 signal only if at this time input E2 enters a logic 0 signal.

Consequently, if input E2 enters a logic 1 signal, the change in the positive polarity pulse signal at input E1 from a 1 to 0, the A output it is not generated.

Let us examine the operation of the differentiating circuit with the implementation of logical functions with a connection to input E1 of an idealised square negative polarity pulse taking into account a change in the signal at input E2 from 0 to 1. (Fig. 8, A).

Let us assume that capacitor C1 is discharged, the inputs E1 and E2 receives logic 0 signals, so at point K the differentiating circuit generates a logic 0 signal.

During t1, input E1 receives signal b, capacitor C1 is charged, at point K a negative polarity pulse is formed in the sequence, as described in point 1.

The capacitor is charged up to the voltage of the logic 1 signal, current in the circuit ceases, at point K a logic 0 signal is generated. During t2, input E2 receives a logic 1 signal. Capacitor C1 is discharged to the logic 0 signal voltage. At point K a logic 1 signal generated. (Capacitor discharge with the connection of logic 1 signal at input E2 is the similar case, when the two capacitor plates are connected to the voltage of one output of the power supply).

During t3, input E1 receives a logic 0 signal, and capacitor C1 is charged up to the logic 1 signal voltage.

A voltage drop from the charge current of capacitor C1 on resistor R1 at point K shapes the positive polarity pulse, whose apex reaches the level of the logic 0 signal voltage. Capacitor C1 is charged up to the logic 1 signal voltage, as a result of which at point K a logic 1 signal is generated .

During t4 input E1 receives a logic 1 signal, and capacitor C1 is discharged. The discharge current of the capacitor on resistor R1 at point K shapes the negative polarity pulse, whose apex reaches the level of the voltage of the doubled logic 1 signal. Capacitor C1 is discharged to the logic 0 signal voltage. At point K we obtain a logic 1 signal.

During t5, input E2 input receives a logic 0 signal, capacitor C it is charged up to the voltage of the logic 1 signal level, as a result of which at point K a logic 0 signal is generated.

During t6, input E1 receives a logic 0 signal. Capacitor C1 is discharged. The capacitor discharge current on resistor R1 at point k shapes the positive polarity pulse in the sequence, described in point 1.

II.3.7. Multivibrator.

The basic master oscillator of the machine operation is a multivibrator, which consists of two cross connected common-emitter amplifiers with capacitive collector-base connections.

To generate the rectangular master clock pulses a multivibrator is used in the self-oscillatory operating mode with a switching frequency of 25 kHz.

The logic symbol and schematic circuit diagram of the multivibrator M214 are given in Fig. 9.

The principle of the self-oscillatory operation of the multivibrator is based on the successive conducting and non-conducting states of transistors T1 and T2.

For the purpose of explaining the self-oscillatory operating mode let us assume that at the given instant transistor T1 is in the conducting state, and that T2 is non-conducting. In the circuit of the conducting transistor a collector current flows from 0V, through T1, R2, -12V, whose value is limited by resistor R2. A small voltage drop occurs in the collector resistance of the conducting transistor. As a result at output A of the multivibrator a logic 0 signal is generated. Simultaneously from 0V through the base-emitter junction of the conducting transistor T1, R4, R1, -12V flows a base current, which creates on base resistance of T1 the small negative potential with respect to the emitter and transistor remains in the conducting state. Let us assume that during the non-conducting state of transistor T1 capacitor C1 charges to the voltage of the logic 1 signal on output A.

After the inversion of the multivibrator transistor T1 is in the conducting state. The left capacitor plate of C1 is connected through the conducting transistor T1 to 0V. The right facing plate through resistors R3 and R1 is connected to -12V. Capacitor C1 is discharged. The discharge current of the capacitor through resistor R7 creates a positive potential on the base of transistor T2 with respect to the emitter and transistor remains in the non-conducting state. Simultaneously capacitor C2 is charged. The left capacitor plate is connected to 0V through the base-emitter of the conducting transistor, the right facing through resistor R5 is connected to the -12V supply. The time constant of capacitor C2's charging circuit has smaller value than the time constant of the discharge circuit of capacitor C1. As a result capacitor C2 is charged for the shorter time interval. The inversion of the multivibrator does not occur until the base of non-conducting transistor T2 has a more positive potential than emitter. The potential of the non-conducting transistors base decreases in proportion to the value of C1's discharge current.

When reaching the insignificant negative potential of the base with respect to the emitter the non-conducting transistor T2 begins to conduct. A positive voltage drop of transistor T2's collector through capacitor C2 enters the base and makes transistor T1 non-conducting, I.E. capacitor C2 begins to be discharged, the capacitor discharge current creates a positive potential on the base of transistor T1, which ensures its non-conducting state.
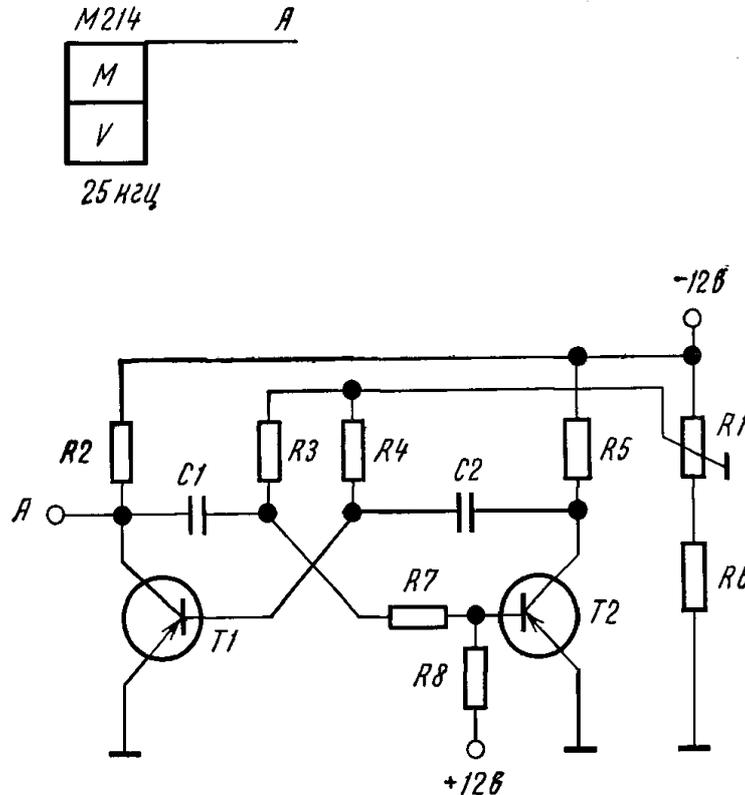

Fig. 9 - Schematic circuit diagram and logic symbol of a multivibrator.

Component parts of M214:

Transistor T1	SB20/2 (2SA15)	β=45–88
" T2	SB20/3 (2SA15)	β=45–88
Capacitor C1	2200pF 10% 63V	
Capacitor C2	2200pF 10% 63V	
Resistor R1	1K (variable)	
" R2	1K 0.05W 10%	
" R3	10K 0.05W 10%	
" R4	10K 0.05W 10%	
" R5	1K5 0.125W 10%	
" R6	1K 0.05W 10%	
" R7	470R 0.05W 10%	
" R8	220K 0.05W 10%	

In turn a negative drop in the voltage of the collector of transistor T1 through capacitor C1 enters the base and boosts the opening of transistor T2. As a result an avalanche transition process of inversion at output A of the multivibrator there occurs a change in the logic signal from 0 to 1.

After setting the multivibrator transistor T2 is in the conducting state, and T1 is non-conducting. Capacitor C2 is discharged and prepares for the following operation of the multivibrator. After sequential inversion at output A of the multivibrator is the pulse shaped of negative floor the steep bank of the polarity.

With the initial start of the multivibrator the +12V supply creates on the base of transistor T2 a more positive potential than that of the base of transistor T1, and ensures the non-conducting state of transistor T2.

After inversion of the multivibrator transistor T2 is in the conducting state. The current of the source of displacement flows in the circuit: +12V, R8, T2, 0V and in practice is not reflected in the value of base current because of the high value of the resistance of resistor R8.

II.3. 8.   Symmetrical trigger (flip-flop).

One of the basic logic elements with memorization is the flip-flop, which consists of two inverters with two collector-base connections. The circuit of a flip-flop has two steady states, which can be characterized as state 0 and 1. In this model of machine adapts the symmetrical not saturated circuit of F119. With the start of the machine the majority of flip-flops are reset into the initial state, which is characterized by the conducting state of transistor T1 and the non-conducting state of transistor T2. In the initial state of a flip-flop a logic 0 signal is generated at output A1, at output A2 a logic 1 signal, which remains until the inversion of the flip-flop originates from the positive polarity pulse, entered at the input of the conducting transistor. After the inversion of the flip-flop transistor T1 is in the non-conducting state, and transistor T2 is conducting. In accordance with the operation of the flip-flop at output A1 a logic 1 signal is generated, and at the output A2 - a logic 0 signal. In this model of machine it is conditionally customary to assume the initial state of a flip-flop as logic 0 and it's working state - as logic 1.

A logic symbol and schematic circuit diagram of the flip-flop F119 are given in Fig. 10.

In the initial state of the flip-flop through the conducting transistor T1 the following current circuit is created: 0V, the resistance of the conducting transistor T1, R2, -12V, whose value in essence is limited by resistor R2. On collector resistor of the conducting transistor a comparatively small voltage drop occurs. As a result the conducting state of transistor T1 generates a logic 0 signal at the A1 output of the flip-flop. The small current of the source of mixing flows in the circuit: +12V, R7, the base-emitter of the conducting transistor T1, 0V. In essence a voltage drop occurs on a comparatively high resistance of resistor R7. A small voltage drop across the base-emitter resistance of the conducting transistor can be disregarded if the opposite base current exceeds by several times the current of the chain of the source of displacement.

Simultaneously from 0V through the base-emitter of the conducting transistor T1, R5, R3, R1, -12V flows a base current, which creates in the resistance of the base of transistor T1 a small
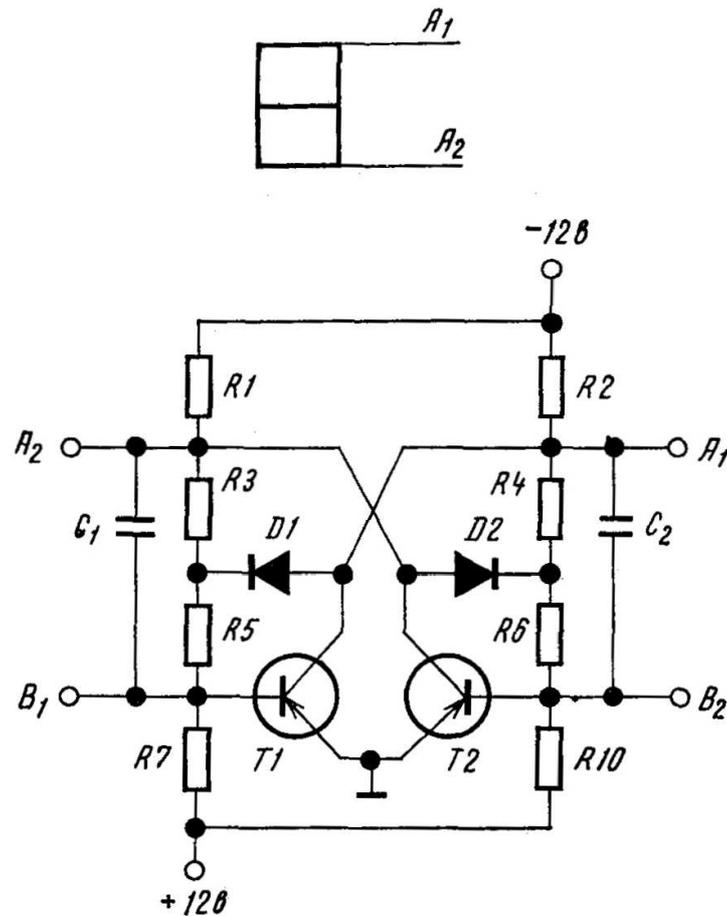

Fig. 10 - Schematic circuit diagram and logic symbol of a flip-flop.

Component parts R 119:

Transistor T1	SA25/2 (2SB75)	β=29-55
" T2	SA25/2 (2SB75)	β=29-55
Diode D1	1N35 or GAZ17	
" D2	1N35 or GAZ17	
Capacitor C1	1000pF 10% 63V	
Capacitor C2	1000pF 10% 63V	
Resistor R1	1K5 0.125W 10%	
" R2	1K5 0.125W 10%	
" R3	10K 0.05W 10%	
" R4	10K 0.05W 10%	
" R5	470R 0.05W 10%	
" R6	470R 0.05W 10%	
" R7	56K 0.05W 10%	
" R10	56K 0.05W 10%	

negative potential with respect to the emitter and retains the transistor in a conducting state. The non-conducting state of transistor T2 is ensured by the voltage of the source of the displacement, whose current flows in the circuit: +12V, R10, R6, R4, the collector-base-emitter of the conducting transistor T1, 0V.

The voltage divider formed from resistors R10, R6 and R4 creates a small positive potential on the base of transistor T2 with respect to the emitter, which retains transistor T2 in the non-conducting state, as a result of which transistor T2 generates a logic 1 signal at output A2. The differentiating chain RC are connected to its inputs for switching the flip-flop from one steady state to another. Let us assume that at input E of the differentiating circuit of the conducting transistor a negative polarity pulse is input. A logic 0 to 1 negative voltage drop of the input signal shapes the negative polarity pulse by the charge current of the capacitor and resistor of the differentiating circuit. The diode of the differentiating circuit is reverse biased, so there is no pulse on the base of the conducting transistor T1. A logic 1 to 0 positive voltage drop on the input signal leads to the capacitor discharging. The discharge current in the differentiating circuit resistor shapes the positive polarity pulse, which opens the diode and is input to the base of the conducting transistor T1. The base of the conducting transistor obtains a positive potential with respect to the emitter, so transistor T1 is non-conducting. On the collector of transistor T1 a negative voltage drop is generated, which enters the speed up capacitor C2 and resistor R4.

At the initial moment the capacitance of C2 shunts base resistors R4 and R6, so a negative drop in the collector voltage of transistor T1 inputs the base of transistor T2. The base of the transistor obtains a negative potential with respect to the emitter, transistor T2 is conducting, on the collector of the transistor is formed a positive voltage drop, which enters the speed up capacitor C1 and resistor R3. At the initial moment the capacitance of C1 shunts the base resistors R3 and R5. A positive voltage drop on the collector of transistor T2 enters the base and boosts the non-conduction of transistor T1. Positive feedback cause an avalanche flow of the switching process of transistors T1 and T2, as a result the flip-flop changes state.

After a flip-flop changes state, the currents flowing in the circuits of the conducting transistor T2, will be analogous to currents previously in the conducting transistor T1. The currents, flowing in the circuits of the non-conducting transistor T1, will be analogous to currents previously in the non-conducting transistor T2.

Diodes D1 and D2 ensure the unsaturated operation of the conducting transistors. For control of a flip-flop in the schematic of the machine, there are three forms of triggering and connection of the differentiating circuits.

Uncontrolled triggering to the bases for separate inputs.

The triggering of flip-flops on the separate inputs is characterized by successive pulse arrival on the inputs E1 and E2 of the differentiating circuits, which ensure the appropriate switching of the flip-flops. The differentiating circuits are connected by the cathodes of diodes to inputs B1 and B2 of a flip-flop, resistors to 0V.

The diodes, connected to the bases of the conducting and non-conducting transistors, obtain the appropriate displacement of cathodes in the direct and opposite direction, which it is unessential for the signals, which are fed to the inputs of the differentiating circuits. From each negative polarity pulse, which entered the inputs E1 and E2, are shaped on the resistor of the differentiating circuit two pulses of different polarity. The negative polarity pulse reverse biases the diode and does not act on the base of the transistor. The positive polarity pulse forward biases the diode and enters the base of transistor. The pulse, which entered the base of the non-conducting transistor, increases the positive potential of base with respect to the emitter and does not change the state of the flip-flop. The pulse, which entered the base of the conducting transistor, creates a more positive potential on the base than on the emitter, which leads to the inversion of the flip-flop.

In the functional diagram of the machine the differentiating circuit, connected to input V1 of the flip-flop, it is customary to assume as the upper lateral input. The differentiating circuit, connected to input V2 of a flip-flop, it is customary to assume as the lower lateral input. The differentiating circuits have the conditional form of pointers in the upper and lower parts of the logic symbol of a flip-flop.

Controlled triggering to the bases for separate inputs.

A difference in the controlled and un-controlled form of triggering the bases consists in the fact that the differentiating circuit diodes obtain the preliminary displacement, as a result of which the trigger pulse can only enter the base of the conducting transistor. For controlled triggering the cathodes of the differentiating circuit diodes are connected to the V1 and V2 inputs, the resistors, correspondingly, to the flip-flop A1 and A2 outputs. In the initial state at output A1 there is a logic 0 signal, whose small negative potential can be ignored. The differentiating circuit diode of preliminary displacement does not obtain. The initial positive polarity peak pulse through the diode enters the base of the conducting transistor. Transistor T1 is non-conducting and causes the inversion of the flip-flop. At output A2 the initial state of the flip-flop outputs a logic 1 signal, which enters the resistor of the differentiating circuit. The anode of the diode obtains preliminary displacement. The diode becomes reversed biased with the logic 1 signal. Pulse shaping with the connection of signal E on input E2 of the differentiating circuit occurs in accordance with the operational description of the differentiating circuit (11.3.6- 2). In accordance with the description the diode remains in the non-conducting state and results in no trigger pulse on the base of the non-conducting transistor. The connection of differentiating chains in the functional diagram of the machine are customarily to assumed as a trigger inputs.

Controlled triggering on the clock input.

The association of two trigger inputs forms a clock input E. Positive polarity trigger pulses ensure the inversion of a flip-flop on the clock input, which only enter the B1 or B2 inputs of a conducting transistor.

Consequently, a negative polarity input pulse on the E inputs of the differentiating circuits cause the required inversion of the flip-flop, the circuit of the controlled starting on the clock input considerably reduces the triggering time of a flip-flop in comparison with the diagram of the uncontrolled starting on the clock input, which can be formed by the association of the upper and lower lateral inputs of a flip-flop, in essence the inversion of a flip-flop with the triggering on the controlled clock input occurs analogously as with the arrival of signal on the separate input. The controlled triggering on the clock input in the functional diagram of the machine is depicted in the form of a pointer, directed to the middle of the side member of the flip-flop logic symbol.

The inversion of a flip-flop can be produced on the static input, the diode of which, whose cathode is connected to the collector of transistor at output A. The anode of diode by input E is under certain conditions connected to 0V (Fig. 8, b). The inversion of a flip-flop on the static (collector) input occurs when a logic 0 signal was sent to the collector of the non-conducting transistor. For as long as the static logic 0 signal is input, the flip-flop is blocked and cannot change its state with trigger pulses on the other inputs. The inversion of a flip-flop on the static input begins from a change in the potential of the collector of the non-conducting transistor, which causes the an avalanche process of the inversion of a flip-flop, the triggering of a flip-flop on the static input is depicted as the section of straight line in the upper or lower part of the logic symbol of a flip-flop.

II.3.9. Monostable multivibrator.

A Monostable, or waiting multivibrator, is a switching monostable circuit, is a single steady state switching circuit that combines the properties of a multivibrator and flip-flop. The initial steady state and the operating temporary steady state can be characterized as the logic states 0 and 1. In this model of the machine the scheme of unsaturated single-vibrator is used. Transistor T1 is conducting in accordance with the initial state, and at the A1 output a logic 0 signal is generated. Transistor T2 is non-conducting, and at the A2 output a logic 1 signal is generated, which remains until the inversion of the monostable, inversion can only occur with the arrival of a positive polarity pulse on the base of the conducting transistor. After the inversion of the monostable output A1 has a logic 1 signal, ant at output A2 a logic 0 signal. After a specific time interval the monostable independently returns to the initial state. Conventionally, it is considered the initial position of a monostable as a logic 0 state and triggered as logic 1.

The logic symbol and schematic circuit diagram of a monostable are given in Fig. 11.
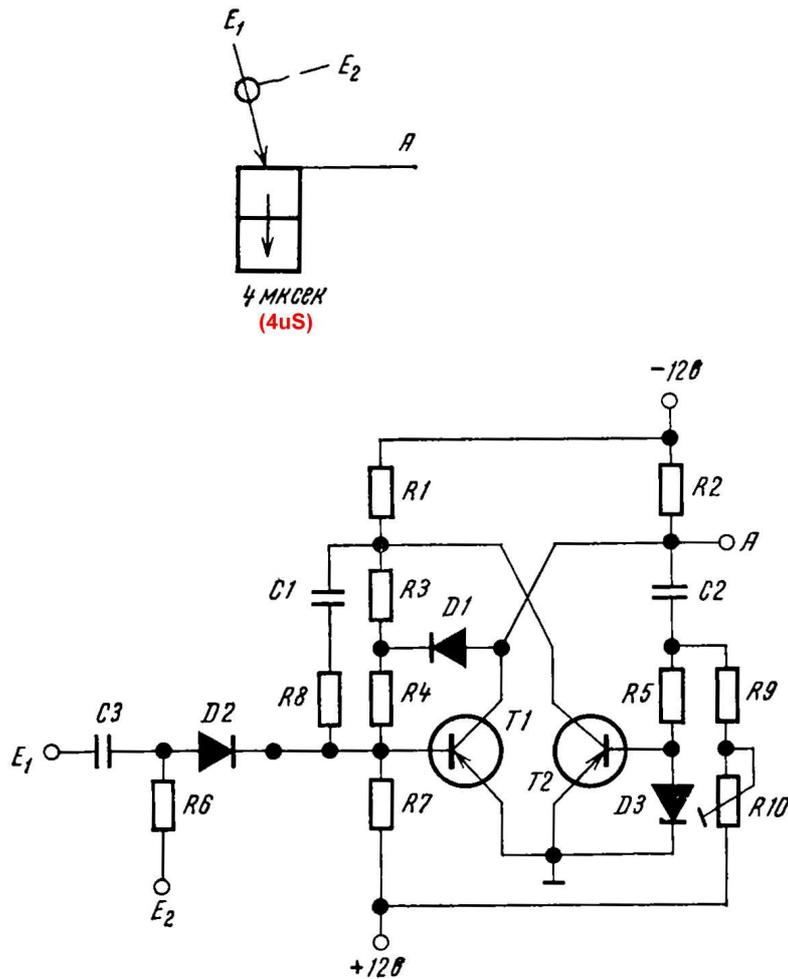
Fig. 11 - Schematic circuit diagram and logic symbol image of a
Monostable (servo multivibrator).

Component parts:

Transistor T1	SB20/3 (2SB75)	β=45-88
" T2	SB20/3 (2SB75)	β=45-88
Diode D1	1N35 or GAZ17	
" D2	1N35 or GAZ17	
" D3	1N35 or GAZ17	
Capacitor C1	220pF 10%	63V
" C2	680pF 10%	63V
" C3	120pF 10%	63V
Resistor R1	1K 0.125W	10%
" R2	1K 0.125W	10%
" R3	10K 0.05W	10%
" R4	470 R 0.05W	10%
" R5	1K 0.05W	10%
" R6	4K7 0.05W	10%
" R7	56K 0.05W	10%
" R8	1K 0.05W	10%
" R9	4K7 0.05W	10%
" R10	50K	(variable)

In the initial state of the monostable through the conducting transistor T1 current flows in the circuit: 0V, resistance of the conducting transistor T1, R2, -12V, whose value in essence is limited by the resistance of resistor R2. In the collector chain of the conducting transistor a small voltage drop occurs on the resistor. The collector potential of transistor T1 is close to the potential of emitter. As a result the conducting state of transistor T1 generates a logic 0 signal at output A of the monostable. A small current from the source of displacement flows in the circuit: +12V, R7, emitter-base of the conducting transistor, 0V. In essence a voltage drop occurs on a comparatively high resistance of resistor R7. The insignificant voltage drop across the emitter-base of the conducting transistor can be disregarded if the base current considerably exceeds the current of the chain of the source of displacement. Simultaneously from 0 V through the base-emitter of the conducting transistor, R4, R3, R1, -12V flows a base current, which creates on the base resistance of transistor T1 a small negative potential with respect to the emitter which retains the transistor in the conducting state. The non-conducting state of transistor T2 is ensured by the voltage of the source of the displacement, whose current flows in the circuit: +12V, R10, R9, R5, D3, 0V. The voltage divider formed from resistors R10, R9, R5 and diode D3 creates a small positive potential on the base of transistor T2 with respect to the emitter due to a voltage drop across the resistance of the forward biased diode. A small positive potential of the base of the non-conducting transistor is also formed due to the current Iko. The positive base potential with respect to the emitter retains transistor T2 in the non-conducting state.

For the inversion of the monostable into the operational order a differentiating RC circuit is connected to the input of diagram.

Input E of the differentiating circuit enters negative polarity pulses, the negative voltage of the logic 1 signal creates a charge current circuit for capacitor C3. The negative polarity pulse is shaped on resistor R6 of the differentiating circuit, the diode of the differentiating circuit is reversed biased, so the pulse on the base of the conducting transistor T1 does not act. After the end of the logic 1 signal input E of the differentiating circuit enters a logic 0 signal, which creates a discharge current in capacitor C3. The discharge current in the resistor the differentiation chain shapes the positive polarity pulse, which enters the base of the conducting transistor through the diode. The base of the conducting transistor obtains a positive potential with respect to the emitter. Transistor T1 is non-conducting, and on the collector of the non-conducting transistor is formed a negative voltage drop, which will enter through the timing capacitor C2 and resistor R5 to the base of transistor T2.

The transistor base obtains a negative potential with respect to the emitter. Transistor T2 is conducting, and on the collector of the conducting transistor is formed a positive voltage drop, which enters the speed up capacitor C1 and resistor R3. At the initial moment the capacitor shunts the base resistors R3 and R4.

A positive voltage drop from the collector of transistor T2 through the speed-up capacitor C1 and resistor R8 enters the base and boosts the non-conducting state of transistor T1. Positive feedback cause an avalanche flow of the process of switching transistors T1 and T2, as a result of which the monostable changes state into the triggered working steady state.

After inversion of the monostable the current of the source of displacement flows in the circuit: +12V, R7, R4, R3, the conducting transistor T2, 0V. The voltage divider formed from resistors R7 and R4, R creates on the base of the non-conducting transistor T1 small positive potential with respect to the emitter, which retains transistor in the non-conducting state. The negative drop in the voltage, which entered the base of transistor T2, reverse biasing diode D3. The capacitor C2 begins to be charged on the chain: 0V, the base-emitter of the conducting transistor T2, R5, C2, R2, -12V, the current of the source of displacement flows in the circuit: +12V, R10, R9, R5, base-emitter of the conducting transistor T2, 0V. At the initial moment the value of current of the charge of the timing capacitor C2 considerably exceeds the value of current of the source of displacement. As a result a voltage drop across the resistance of the conducting transistor from the current of charge exceeds the value of a voltage drop from the current of the source of displacement. On the base of the conducting transistor negative potential with respect to the emitter, which retains transistor T2 in the conducting state, is created. The reactance X, of capacitor C2 increases in proportion to charge, the current of charge decreases, the potential of base becomes more positive. With reaching of the small positive potential of base with respect to the emitter transistor T2 is non-conducting. A negative drop in the voltage on the collector of transistor T2 causes an avalanche-type process of the inversion of the monostable into the initial state.

The operation of a monostable can be presented as follows. After triggering the monostable the -12V supply charges capacitor C2, through resistor R5, the base-emitter of the conducting transistor T2, and in parallel through resistors R9, R10 to the positive poles of the ±12V power supplies, as a result of the electron concentration on the base of the conducting transistor is created a specific negative potential, which keeps transistor T2 in the conducting state. The current in the base circuit transistor T2 decreases in proportion to the charge on capacitor C2, the potential of base becomes positive with respect to the emitter and making transistor T2 non-conducting, which ensures the reversion of the monostable into the initial state. Diode D1 ensures that transistor T1 operates in an unsaturated condition. The variable resistor R10 adjusts the current value of the source of displacement and so the duration of the working order of the monostable.

II.3.10.   "Minus" sign driver.

Amplifier V700 drives an incandescent lamp, whose illumination ensures the display of "minus" sign. The logic symbol and the schematic circuit diagram of the "minus" sign display amplifier are given in Fig. 12.

In the initial state input E of the amplifier receives a logic level 0 signal from the MZ output of the sign flip-flop.

In the circuit: 0V, R1, R2, +12V - flows the small current, whose value is limited by the total resistance of the voltage divider resistors R1 and R2 (110 kilohms).
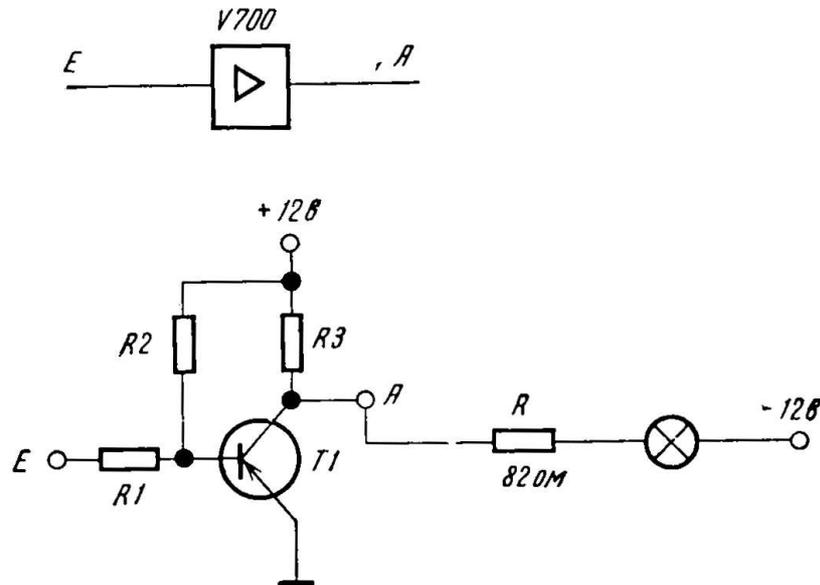

Fig. 12 - Schematic circuit diagram and logic symbol
of the "minus" indicator lamp.

Component parts of V700:

Transistor T1	SA250/4 (2SB77)		β=72-166
Resistor R1	10K	0.05W	10%
" R2	100K	0.05W	10%
" R3	1K2	0.5W	10%

A voltage drop across resistor R1 creates on the base of transistor T1 positive potential in the range of +1,2 V and ensures the non-conducting state of transistor.

Simultaneously into the chain: +12V, R3, 82 ohm resistor, indicator lamp, -12V supply, a current of 17ma flows which is insufficient to make the incandescent lamp illuminate. (The voltage between the power supplies is equal to 24V, the resistance of the circuit - approximately 1,3 kilohms.)

A voltage drop across the incandescent lamp and 82ohm resistor creates a negative potential on the collector of the transistor in relation to the emitter near to -10V.

As a result transistor T1 is non-conducting according to diagram with general emitter.

After setting the sign of the number flip-flop into the working state input E of the amplifier receives a logic 1 signal. A voltage drop across resistor R2 from the circuit current of the voltage divider resistors R1 and R2 creates a negative potential on the base with respect to the emitter. Transistor T1 is conducting. This is analogous with the description of the operation of the inverter the current of the voltage source, flowing in the circuit: +12V, R2, the base-emitter of the conducting transistor, 0V - will be considerably less than the opposite current in the base, flowing for the chain: 0V, the base-emitter of the conducting transistor, R1, the signal source internal resistance, -12V. The resulting current creates a voltage drop across the base-emitter resistance of the conducting transistor and ensures the negative potential on the base of transistor T1.

Simultaneously in the circuit: 0V, base-emitter, conducting transistor collector, 82 ohm resistor, incandescent lamp, -12V - flows a current, whose value ensures the illumination of the incandescent lamp.

Current in the incandescent lamp circuit is determined by the resistance of the chain, which can be considered approximately equal to 100 - 120 ohms.

Consequently, the value of current, flowing through the lamp, is within the limits 100 - 120ma.

After the end of the logic 1 signal input E of the amplifier circuit receives a logic 0 signal. Transistor T1 is turned off, and illumination of the incandescent lamp ceases.

II.3.11. Digital display cathode driver.

Amplifier V701 connects the numerical cathodes of the display to the -90V supply. In the initial state input E of amplifier receives a logic 1 signal. Output A of the amplifier generates logic 0 signal (U_{A0}), which prevents the illumination of the numerical cathodes. When input E of the amplifier receives a logic 0 signal, output A of the amplifier generates a -Ua (-90V) signal, which enters the appropriate numerical cathode and ensure the illumination of the appropriate number with a simultaneous connection of the digital lamp anode to the $+U_A$ (+100v) voltage.

The logic symbol and schematic circuit diagram of the numerical cathode amplifier V701 are given in Fig. 13.

The amplifier is assembled from *n-p-n* transistors. The transistor emitters are simultaneously connected to the $-U_A$ (-90V) power supply and to the divider of the voltage source $-U_N$ (-12V). The collector resistor R2 is connected to U_A, (0V of sources $-U_A$, $+U_A$).

It is necessary to keep in mind, that the operation of *n-p-n* transistor types in comparison with *p-n-p* transistors uses the opposite polarity of signals.

A voltage drop across resistor R21 in the circuit of the voltage divider formed from resistors R20, R21 of the -12V power supply determines the emitter potential of transistor T1. With respect to the base the emitter potential is -10V.

In the initial state input E of the amplifier inputs a logic 1 signal from the output of an inverter, which is within the limits -11,5V. As a result the base of the transistor obtains negative potential with respect to the emitter and ensures the non-conducting state of the transistor. Output A of the amplifier circuit generates a logic 0 signal (U_{A0}), which enters the appropriate cathode of a digital indicator tube.

A logic 0 signal at input E of the amplifier creates a positive potential of the base with respect to the emitter.

Transistor T1 is conducting. Collector current in the circuit: 0V (U_{a0}), R2, T1, -U_A (-90V) of the conducting transistor with the illuminated indicator light is limited by the value of resistor R2. Simultaneously the current, flowing in the circuit: signal source 0V, R1, base-emitter of the conducting transistor T1, R20 of the power supply, (-12V) creates a positive potential on the base of the transistor with respect to the emitter and ensures the conducting state of the transistor until input E of the circuit becomes a logic 0 signal.

A voltage drop across the resistance of the conducting transistor from the collector current can in practice be ignored.

As a result the conducting state of transistor T1 generates a signal -U_a (-90V) at output A, which enters the appropriate cathodes of the digital indicator tubes.

Fig. 13. Schematic circuit diagram and logic symbol of the display cathode driver.

Elements of diagram V701:
Transistor T1   BSY79   β>30
Resistor R1   12K   0.05w 10%
   » R2   100K   0.25w 10%

At the end of the logic 0 signal input E of the amplifier circuit receives a logic 1 signal which creates a negative potential of the base with respect to the emitter of transistor T1.

Transistor T1 becomes non-conducting, and from output A of the signal amplifier 0 (U_{A0}) enters the corresponding cathode of cathode of the digital indicator tubes.

II.3.12.   Digital display Anode driver.

The two-stage amplifier V703 serves to connect the anodes of the digital indicator lights to the +Ua (+100V) voltage supply. In the initial state input E of the amplifier receives a logic 0 signal. From output A of the signal amplifier a logic 0 (U_{A0}) enters the anode of a digital indicator tube and prevents the illumination of the cathodes.
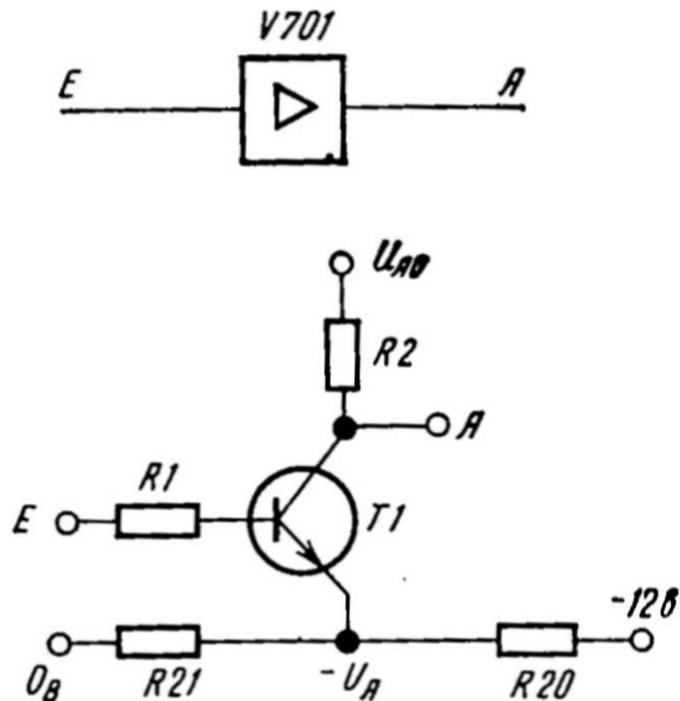
When input E of the amplifier receives a logic 1 signal, output A of the amplifier generates a +Ua (+100V) signal, which enters the anode of an indicator tube and ensures the illumination of the corresponding numerical cathode with the simultaneous connection of that cathode to the -90V supply voltage.

Logic symbol and schematic circuit diagram of the anode driver V703 are given in Fig. 14.
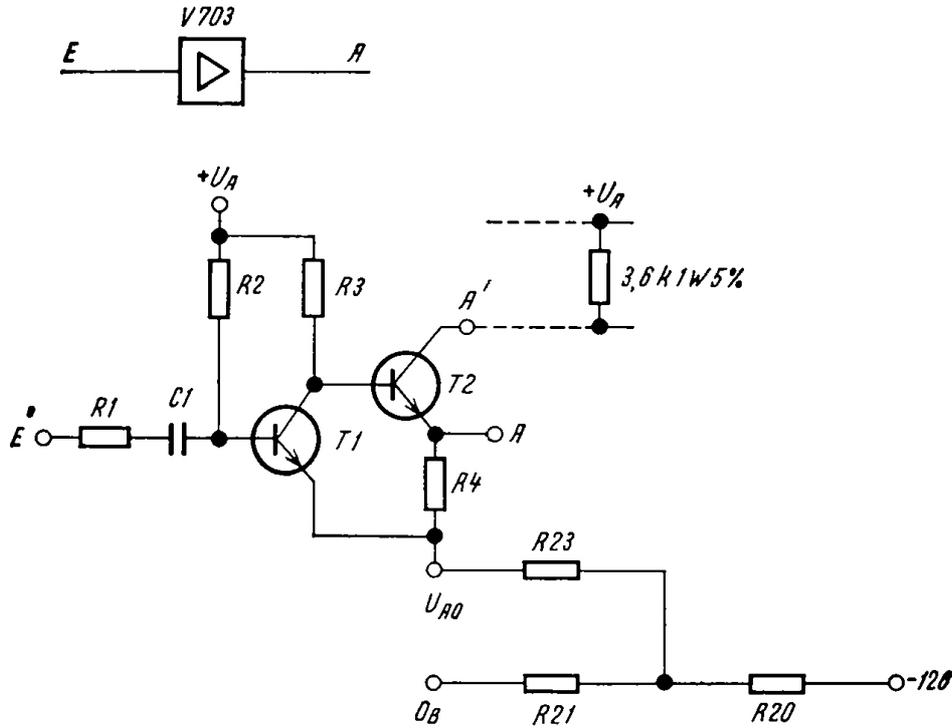

Fig. 14 Schematic circuit diagram and logic symbol of the
digital display anode driver.

Elements of diagram V703:

Transistor T1	BSU70		$\beta > 30$
Transistor T2	BSU70		$\beta > 30$
Capacitor C1	0.22uF	20%	160V
Resistor R1	4K7	0.05W	10%
" R2	1K	0.05W	10%
" R3	68K	0.25W	10%
" R4	100K	0.125W	10%

The amplifier is assembled with *n-p-n* type transistors. The transistor emitters are all connected to the output of the U_{A0} (0V of the sources - U_A, $+U_A$) voltage source, also, through resistor R23 to the divider of the voltage of the power supply $-U_N$ (-12V). The collector resistors are connected to $+U_A$ (+100V).

In the initial state input E of the amplifier receives a logic 0 signal. The power supply voltage $+U_A$ (+100V) through resistor R2 enters the base and turns on transistor T1. Current, flowing in the circuit: $+U_A$, R2, base-emitter of the conducting transistor, 0V (U_A) - creates on the base a small positive potential, with respect to the emitter, which ensures the conducting state of transistor T1.

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In the circuit: 0V (U_{A0}), T1, R3, $+U_A$ flows a collector current, whose value in essence is limited by the resistance of resistor R3. An insignificant voltage drop across the resistance of the conducting transistor T1 can be ignored and to consider that the logic 0 signal from the collector of transistor T1 enters the base and ensures the non-conducting state of transistor T2. At output A of the amplifier circuit a logic 0 (U_{A0}) signal is generated, which enters the anode of the corresponding indicator tube. The emitter of transistor T1 through resistor R23 is connected to the voltage divider formed from resistors R20 and R21, and the power supply -12V.

At input E of the amplifier circuit a logic 1 signal is entered through resistor R1 and the isolating capacitor C1 entering the base and making transistor T1 non-conducting.

A positive potential with respect to the emitter is created on the base of transistor T2 so transistor T2 is conducting. Collector current in the circuit of: $+U_A$ (+100V), 3,6k resistor, T2, R4, 0V (U_{A0}) of the conducting transistor with the illuminated state of the indicator light is limited by the 3,6k and R4 resistors. In comparison with resistor R4 a small voltage drop across the 3,6k resistance ensures at output A a signal of approximately +96V, which enters the anode of the corresponding digital indicator light. The current, flowing in the circuit of: 0V (U_{A0}), R4, T2, R3, $+U_A$ (+100V), creates on the base a positive potential, which ensures the conducting state of transistor T2 until transistor T1 is in the non-conducting state.

In proportion to the charge on capacitor C1 the base obtains a positive potential with respect to the emitter and conducts transistor T1, as a result transistor T2 is non-conducting, and at output A of the driver a logic 0 (Ua0) signal is generated.

The simultaneously conducting state of transistor T1 (diagram V701) and T2 (diagram V703) produces the circuit feeding the voltages -90v and +100v to the cathode and anode of the corresponding indicator light.

The applied voltage creates the ignition of an indicator light and resultant current in the circuit: $+U_A$ (+100V), 3,6 kilohms resistor, T2, anode-cathode of an indicator light, T1, U_A (-90V).

The value of current in the circuit in effect will be limited by the 3,6k resistor and by the internal resistance of the indicator light.
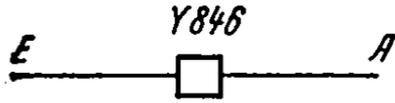
II.3.13.   Keyboard filter diagram.

Connection diagrams Y846 and Y846/1 ensure the connection between the electronic arithmetic-logic unit and the electromechanical keyboard input unit. The basic task of the diagrams is to control the operation of the differentiating circuits.

Logic symbol and schematic circuit diagram V846 are given in Fig. 15.

In the initial state input E of the keyboard filter diagram no signals are apparent through the dead contacts of the keyboard.

At output A of the keyboard filter circuit a logic 1 signal is generated, capacitor C1 is charged to the voltage of the power supply. After closing of the corresponding keyboard contact a logic 0 signal enters input E of the keyboard filter. A small voltage drop occurs across resistor R1 from the current, flowing in the circuit of 0V, R1, R2, -12V, as a result of this output A of the keyboard filter generates a logic 0 signal.

Capacitor C1 serves to smooth the signal pulses from the mechanical microswitch contacts of the input unit.
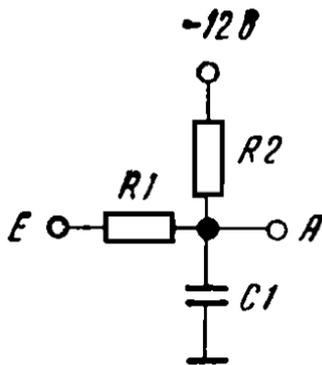
Fig 15. Schematic circuit diagram and logic symbol of the keyboard connection diagram.

Elements of diagram Y846:

Capacitor C1	0,047uF	63V
Resistor R1 100R	0.05w	10%
" R2 10K	0.05w	10%

In the functional diagram of the machine outputs A of the keyboard filter diagrams in essence are connected to the controlling outputs E2 of the differentiating circuits.

In the keyboard filter diagrams for circuits Y846/1 resistor R1 is absent.

II.3.14. Schmitt trigger.

The operational sequence of a Schmitt trigger has much in common with the operational regime of the servo multivibrator. In the initial state from the outputs of the keyboard filters, logic 1 signals ensure the reversed biased state of the diodes at input E of the Schmitt trigger circuit. The reversed biased state of the diode in practice does not have an effect on the currents of the initial state of the Schmitt trigger.

In the initial state of the Schmitt trigger output A generates a logic 1 signal.

With the operation of digital or functional keys from the output of the corresponding keyboard filter there is entered a logic 0 signal, which opens one of the steering diodes of the Schmitt trigger.

The transition of the Schmitt trigger into the working state proceeds in 10ms from a logic 0 input signal, which enter through one of the forward biased diodes of input E of the circuit diagram. In its operated state the Schmitt trigger generates a logic 0 signal at output A until input E enters a logic 0 signal.

After the end of the logic 0 signal from the output of the keyboard filters a logic 1 signal is input to the appropriate steering diode of the Schmitt trigger, which reverse biases the diode and ensures the automatic transition of the Schmitt trigger into the initial state.

Logic symbol and schematic circuit diagram of the Schmitt trigger are given in Fig. 16.

In the initial state of the Schmitt trigger schematic transistor T1 is in the unearthed state.

Transistor T2 is non-conducting, so output A of the Schmitt trigger circuit is generates a logic 1 signal.
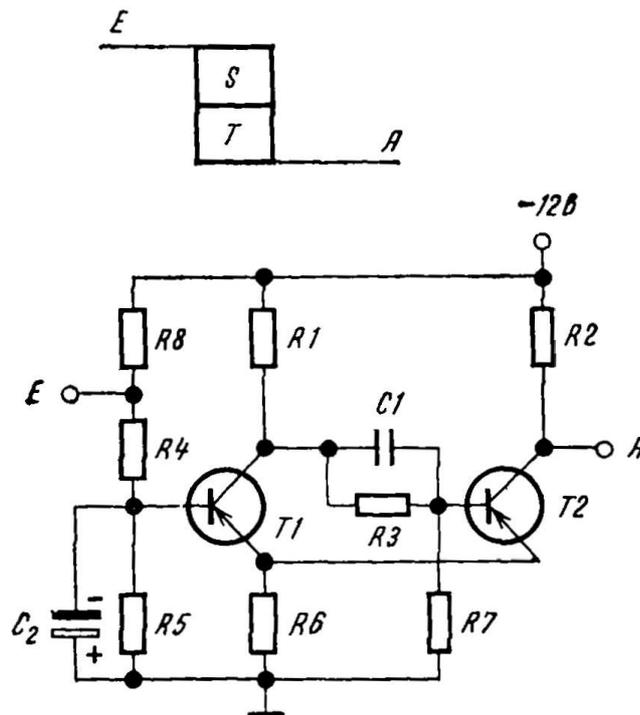
Fig. 16. Schematic circuit diagram of the Schmitt trigger.

Component parts:

Transistor T1	SA25/2 (2SB75)		B=29-55
Transistor T2	SA25/2 (2SB75)		B=29-55
Capacitor C1	2,700pF	10%	63V
" C2	20uF	15%	63V
Resistor R1	1K8	0.125W	10%
" R2	1K5	0.125W	10%
" R3	128K	0.05W	10%
" R4	3K9	0.05W	10%
" R5	2K7	0.05W	10%
" R6	47R	0.05W	10%
" R7	4K7	0.05W	10%
" R8	2K2	0.05W	10%

After application at input E of a 0V feed signal voltage through resistors R5, R4, R8 and in parallel R7, R3, R1, currents are created in these voltage divider circuits.

A voltage drop across resistor R5 of the voltage divider creates on the base of transistor T1 a negative potential with respect to the emitter. Transistor T1 is conducting.

In the circuit 0V, R6, T1, R1, -12V of the conducting transistor flows collector current, whose value in essence is limited by the resistance of resistor R1. On the collector of the conducting transistor a small negative potential is created, which is determined by the value of a voltage drop across resistor R6 and the resistance of the conducting transistor T1.

Simultaneously through in the circuit: 0V, R6, the base-emitter of transistor T1, R4, R8, -12V of the conducting transistor - flows base current. A voltage drop across the base-emitter resistance of the conducting transistor creates a negative potential at the base with respect to the emitter and ensures the conducting state of transistor T1. Capacitor C2 is charged up to the value of a voltage drop across resistor R6 and the resistance of the base-emitter of the conducting transistor T1.

A voltage drop across resistor R6 creates a negative potential at the emitter with respect to the base and ensures the non-conducting state of transistor T2.

Taking into account the small negative potential of the collector at the conducting transistor T1, a voltage drop across resistor R7 in the circuit of the voltage divider formed from resistors R7, R3, R1 creates on the base of transistor T2 the respectively small negative potential, which enters the base of transistor T2.

The base has more positive potential with respect to the emitter, as a result of which transistor T2 is in the non-conducting state. With the entry of a logic 0 signal from a corresponding keyboard filter circuit through the forward biased diode the signal enters input E of the Schmitt trigger circuit, and the charged capacitor C2 begins to be discharged through parallel connected resistors R4 and R5. A voltage drop from the resultant capacitor discharge current on resistors R4 and R5 ensures the negative potential of the base and the conducting state of transistor T1.

AS current in circuit and voltage drop across resistors R4 and R5 decreases in proportion to the capacitor discharge, the potential of the base becomes more positive, as a result transistor T1 begins to be non-conducting ensuring the inversion of the Schmitt trigger into the working order. Current in the collector circuit decreases, and the potential of the collector becomes more negative and through the rising capacitance of C1 it inputs the base of transistor T2. As the voltage drop across resistor R6 decreases, the potential of the emitter of transistor T2 becomes more positive.

Transistor T2 is conducting, in the 0V, R6, T2, R2, -12V circuit of the conducting transistor flows collector current, whose value in essence is limited by resistor R2. A logic 0 signal is generated at output A of the Schmitt trigger circuit. Simultaneously through the conducting transistor in the circuit: 0V, R6, the base-emitter of transistor T2, R3, R1, -12V - flows base current.

A voltage drop across resistance of the base-emitter of the conducting transistor creates the negative potential of the base with respect to the emitter and ensures the conducting state of transistor T2. A voltage drop across resistor R6 creates a negative potential at the emitter with respect to the base and ensures the non-conducting state of transistor T1.

After the end of the logic 0 signal the appropriate steering diode of the circuit diagram enters a logic 1 signal. Transistor T1 is conducting in the sequence, analogous to the description, and ensures the inversion of the Schmitt trigger into the initial state.

11.3.15. Ferrite core polarity reversal drivers.

The diagram of drivers Y910, Y911, Y912 show the polarity reversal system of the ferrite core storage. The polarity reversal of a ferrite core is ensured by the simultaneous operation of 4 drivers, which create the polarity reversal current of Im. Each pair of drivers creates a half-current $\frac{Im}{2}$ of the polarity reversal Im.

Two half-currents $\frac{Im}{2}$, those simultaneously taking place through the ferrite core, create a current Im, which ensures the polarity reversal of a ferrite core, I.e. reading or writing of an information bit.

Half-currents $\frac{Im}{2}$, but not coinciding in time, do not produce a polarity reversal of a ferrite core.

A logic symbol and schematic diagram of drivers Y910, Y911 are given in Fig. 17.

The shaping of the half-current pulses $\frac{Im}{2}$ ensures the sequential connection of the second steps of two drivers of polarity reversal.

Connection A2 of the second driver Y910 is connected to 0V (-Usp) of the memory unit power supply.

Connection A1 of the second driver Y910 is connected by one of the wires (register read or discharge, register write or discharge), which routed through the ferrite cores, is connected to connection A2 of the second driver Y911.

Connection A1 of the second driver Y911 through a 40R (3 X 120R) resistor is connected to the memory unit power supply negative (-Usp).

In the initial state inputs E of the first set of drivers from outputs A of the AND gates receive logic 0 signals. The current from the source of displacement flows in the circuit: +12V, R2, R1, 0V. A voltage drop across resistors R1 creates a positive potential on the bases and ensures the non-conducting state of transistors T1 of drivers Y910, Y911.

In the collector circuit of the non-conducting transistor T1 a current Iko flows through the primary windings of the transformers. In the secondary windings of the transformers an EMF is not induced, so transistor T2 are in the non-conducting state. The emitter junctions of transistor T2 are shunted by the small resistance of the secondary windings of the transformers, a result of which is that the series connection of the transformers can be considered practically as a series connection of diodes, to which is connected an inverse voltage.

After the inversion of the monostable or Kipp oscillator (German "*kippen*") into the working order through two series connected inverters and the corresponding AND gate E inputs of first stages of cascades enters a negative polarity pulse with a duration of 4uS.
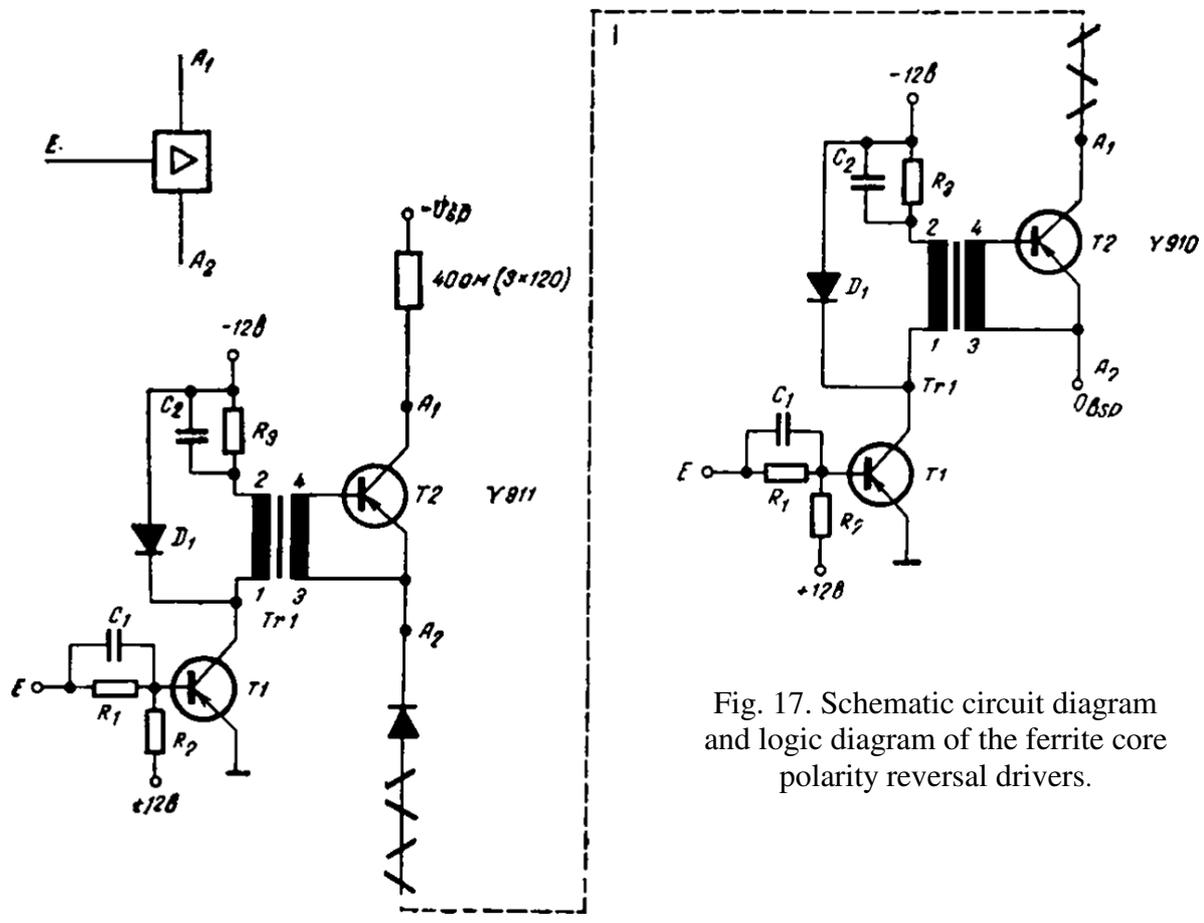

Fig. 17. Schematic circuit diagram and logic diagram of the ferrite core polarity reversal drivers.

Component parts	V910	V911	V912
Transistor T1	SB20/4 (2SA17) β = 72-166	SB20/4 (2SA17) β = 72-166	SB20/4 (2SA17) β = 72-166
"T2	SC20/3 (2SB210) β = 45-88	SC20/3 (2SB210) β = 45-88	SC20/4 (2SB210) β = 72-166
Diode D1	OA741	OA741	OA741
Capacitor C1	220nF 10% 63V	220nF 10% 63V	220nF 10% 63V
" C2	330nF 10% 63V	330nF 10% 63V	330nF 10% 63V
Resistor R1	12K 10% 0.05W	12K 10% 0.05W	12K 10% 0.05W
" R2	68K 10% 0.05W	68K 10% 0.05W	68K 10% 0.05W
" R3	820R 10% 0.125W	820R 10% 0.125W	820R 10% 0.125W
Transformer TR1	TR910	TR910	TR912

At the initial moment capacitors C1 shunt resistors R1, the negative voltage input signal enters the bases and cuts off transistor T1. In the circuit: 0V, T1, the primary winding of the transformer, C2, -12V of the collector of the conducting transistor, current flow begins.

At the initial moment capacitor C2 shunt the collector resistor R3, and the primary winding of the transformer will have a high inductive reactance X_L.

In the collector circuit through the primary winding flows a minimum current, whose value grows exponentially with a time constant $t = \dfrac{L}{R}$.

From a change of the current in the primary winding of the transformer an EMF is induced in the secondary winding, the negative pole of which is applied to the base and the positive to the emitter of transistor T2.

Transistor T2 is conducting. In the circuit of the conducting transistor: 0V (0vsp) through T2 of the cascaded amplifier Y910, the wire through the ferrite cores, T2 of the cascaded amplifier Y911, the 40R (3 X 120) resistor on -Usp, a current flow $\dfrac{Im}{2}$ begins, whose value is limited to 0,25A.

After the end of the logic 1 signal, the E inputs of transistor T1 receive logic 0 signals.

Transistor T1 is non-conducting. Current in the collector circuit decreases exponentially with a time constant T. From a change of the current in the primary winding of the transformer in the secondary winding is induced an EMF, the negative pole of which is applied to the emitter and the positive to the base of transistor T2. As a result of the changes in the polarity of the voltage on the outputs of the secondary winding transistor T2 is non-conducting, I.E. extinction of the self-induced EMF of the transformer primary winding occurs through capacitor C2 and diode D1.

II.4.   POWER UNIT.

The machine power unit consists of seven power supplies:
1) Stabilized supply voltage -U_n, used in the arithmetic-logic unit as –12V;
2) Stabilized supply voltage –Usp, used in the memory unit -11,5 ÷ -13,56V (depending on temperature);
3) Stabilized voltage +Up, used in the arithmetical and memory unit of +12V;
4) Non-stabilized supply voltage –Ua, the cathodes of digital lamps –90V;
5) Non-stabilized supply voltage of +Ua, of the anodes of the digital lamps +100V;
6) Non-stabilized supply of alternating voltage for the indicator light of ~110V;
7) Autonomous power for the electronic voltage regulation circuit with overloads and short circuit.

11.4.1.   Principle of electronic voltage regulation.

The basis of the electronic regulating circuit is assumed the specific reference voltage of the comparator device. A reference voltage is created as a result the internal change of the resistance of Zener diode ZD2 (Fig. 18).
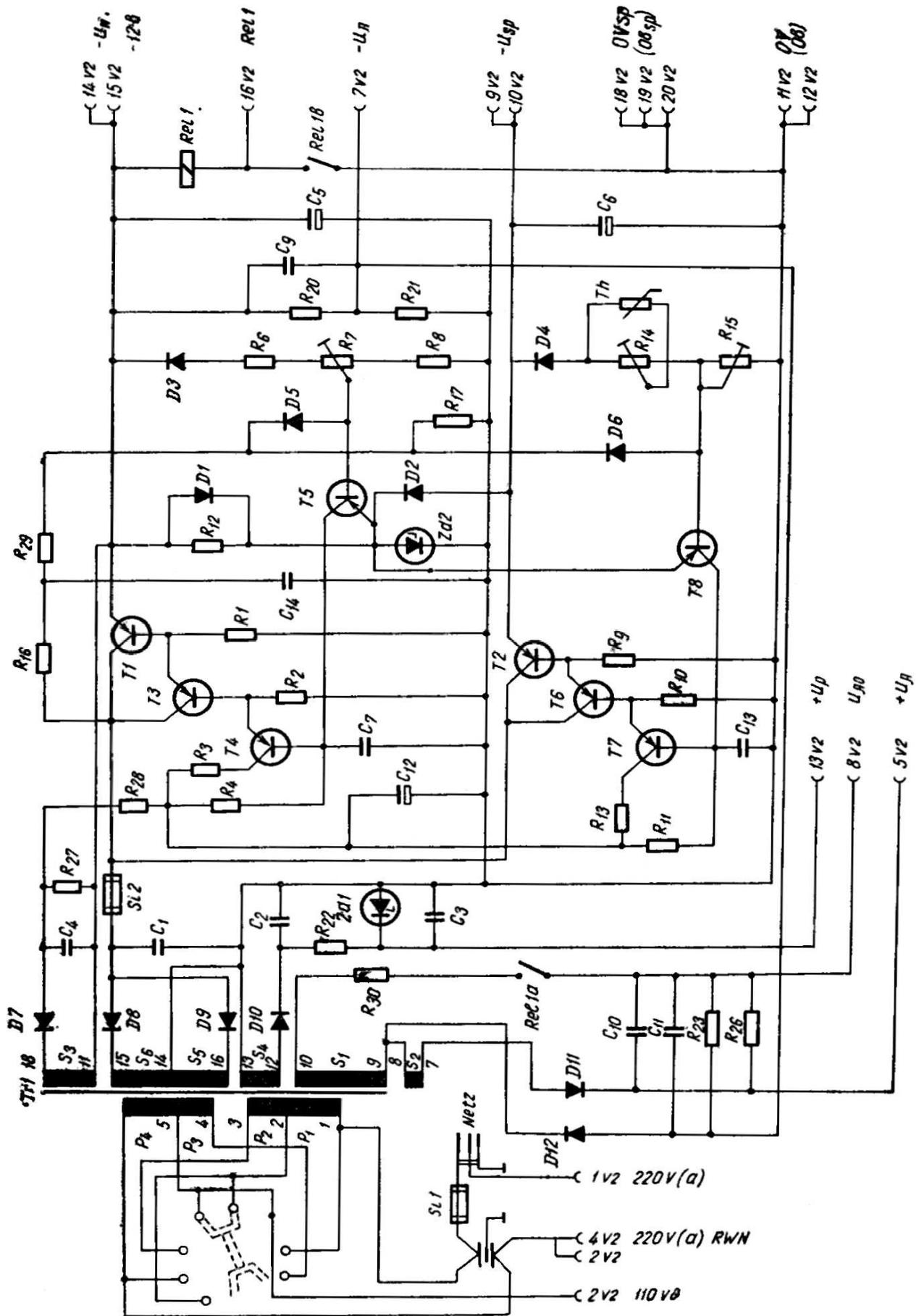
Fig 18.   Power supply electrical circuit diagram.

A larger or smaller change of the current value in the regulator circuit causes an appropriate reverse change of the internal resistance of the regulator into a smaller or large value. As a result the voltage the drop across the regulator is constant, with respect to the reference voltage and comparator input voltage from variable resistor R7. Transistor T5 performs the functions of a comparator device. Input voltage is compared with the reference voltage and changes the voltage on the output of the power supply. A smaller or larger change in the voltage on the output of the power supply produces an appropriate change of current in the circuit of the voltage divider formed by resistors R8, R7, R6 and the input voltage of the comparator. The comparator inverts the signal phase, which through the DC amplifier formed by transistors T4, T3 is fed to the input of the regulating element. Transistor T1 performs the functions of the regulated element. The internal resistance of the regulating transistor varies to a larger or smaller amount and ensures the assigned voltage value on the output of the power supply.

11.4.2. Rectification of power supplies -U_N and -U_{sp}.

Rectification of the power -U_N and -U_{sp} supplies is performed by a full-wave rectifier circuit with centre tap and operates on the load with the capacitive reaction. After switching on the mains voltage supply by turning the disk of the mains switch AUS - EIN, an alternating current begins to flow in the primary winding of the transformer. An alternating voltage is induced in the secondary windings S5, S6 of the transformer, which enter diodes D8 and D9. Smoothing of the rectified supply is carried out by capacitor C1 which is connected in parallel to the working load of the rectifier. At supply switch on the resistance of the working load is shunted by a discharged filter capacitor. The induced voltage of the secondary winding through the rectifier diodes D8 and D9 create a charge current in capacitor C1. As capacitor C1 is charged, the reactance X_C, of C1 increases, and the charge current of the chain decreases, voltage on the output of the rectifier increases. Capacitor C1 charges almost to the amplitude value of the rectified voltage. The resistance of the working load is connected to the circuit of the transformer secondary winding.

Let us assume that in the positive half-period of the transformer secondary windings output 15 has a positive potential, and output 16 a negative potential relative to the centre tap at output 14. During the positive half-period diode D9 is connected to the forward voltage of the second-half of the transformer secondary winding. Diode D9 is forward biased. In the circuit: secondary winding output 16, diode D9, load resistance, output of the transformer secondary winding 14 - flows a current, whose value is limited by the resistance of the switched on load.

Simultaneously diode D8 is connected to the inverse voltage of the complete transformer secondary winding, which retains diode in the reversed biased state.

In the negative half-period the transformer secondary winding output 16 has a positive potential, and output 15 - a negative value relative to the centre tap at output 14.

During the negative half-period diode D8 is connected to the forward voltage of the first half of the transformer secondary winding. In the circuit: transformer secondary output winding 15, diode D8, load resistance, transformer secondary output winding 14 - flows a current, whose value is also limited by the resistance of the switched on load. Simultaneously diode D9 is connected to the inverse voltage of the complete transformer secondary winding, which retains diode in the reversed biased state.

During each half-period in proportion to an increase in the sinusoidal voltage, when the potential of the cathode becomes more negative than the potential of the negative plate of capacitor C1, one of the diodes is forward biased. In one half of the transformer secondary winding circuit flows a current, through the parallel connected capacitor C1 and the corresponding resistance of the switched on load. In proportion to the decrease in the sinusoidal voltage, when the potential of cathode becomes more positive than the potential of capacitor plate, the diode is reversed biased, and capacitor discharge current flows through the load resistance in the same direction, the decrease of voltage on the capacitor plate C1 is proportional to the value of discharge current, which is restored in proportion to the capacitor discharge during each half-period. Alternation of the charge and discharge cycles capacitor C1 ensures the smoothing of the pulsed voltage on the output of the rectifier

In turn the rectified voltage ensures the operation of the voltage regulating circuit elements and nourishment of the connected load.

One should consider during the replacement of diodes that the reversed biased diode voltage is under the voltage of the complete secondary winding of the transformer, which is equal to double the voltage of the rectified voltage.

11.4.3. Stabilized supply voltage -12V (-U_N).

Let us assume that on the output of the power supply the -12V supply is established, and in the circuit: 0V, R8, variable resistor R7, R6, D3, -12V - a current flows, a voltage drop across resistor R8 and variable resistor R7 determines the potential of the base of transistor T5 in to relation to the emitter. Transistor T5 in the voltage regulating circuit fulfils the functions of the comparator device of the stabilized voltage of the emitter and non-stabilized voltage of the base, which changes response to the voltage on the output of the power supply.

When the established working voltage on the output of the power supply does not change, the base of transistor T5 has a more negative potential than the emitter, and ensures its operation in an unsaturated regime. With half-wave rectification from diode D7, resistors R27, R28 and capacitor C4, fulfils a smoothing function, and forms a negative supply of autonomous power, to which are connected resistors R3, R4 and the collectors of transistors T4 and T5.

Transistor T5 is in the conducting state, and through the conducting transistor a collector current flows in the circuit: 0V, the Zener diode ZD2, T5, R4, R28, negative supply of autonomous power.

A voltage drop across Zener diode ZD2 and the conducting transistor T5 ensures the negative potential of the base with respect to the emitter of transistor T4. Transistor T4 completes the function of the first stage of a feedback amplifier and it is in the non-conducting unsaturated state.

In the conducting transistor T4 a collector current flows in the circuit: 0V, R2, T4, R3, R28, negative supply of autonomous power. A voltage drop across resistor R2 ensures the negative potential of base with respect to the emitter of transistor T3. Transistor T3 completes the function of the second stage of the feedback amplifier and it is in the non-conducting unsaturated state.

Through the conducting transistor T3 a collector current flows in the circuit: 0V, R1, T3, negative of the power supply rectifier. A voltage drop across resistor R1 ensures the negative potential of base with respect to the emitter of transistor T1.

Transistor T1 completes the function of the regulated element as a variable resistor and it is in the non-conducting unsaturated state, the given quantity of the internal resistance of transistor T1 according to the allowed conditions ensures the -12V output of the power supply.

A decreasing change in the output voltage of the power supply produces the appropriate current change in the voltage divider circuit on the base of transistor T5. The voltage drop across resistor R8 and variable resistor R7 decreases. The potential on the base of transistor T5 becomes more positive and somewhat makes the transistor non-conducting. The internal resistance of transistor increases, current in circuit and voltage drop across the collector resistor R4 decreases. The collector potential of transistor T5, and also the base of transistor T4 becomes more negative and somewhat further opens transistor T4, the internal resistance of the transistor decreases, so current in the circuit and voltage drop across the emitter resistor R2 increases. The emitter potential of transistor T4, and also the base of transistor T3 become more negative and so further opens transistor T3, the internal resistance of the transistor decreases, current in the circuit and voltage drop across the emitter resistor R1 increases. The emitter potential of transistor T3, and also the base of transistor T1 becomes more negative and so further opens transistor T1.

The internal resistance of transistor T1 decreases, the emitter potential becomes more negative, as a result of which the -12V on the output increases to the assigned value.

When an increasing change in the output voltage on the power supply occurs, an appropriate change of current in the voltage divider circuit on the base of transistor T5 occurs, voltage drop across resistor R8 and variable resistor R7 increases. The base potential becomes more negative and further opens transistor T5. The internal resistance of transistor decreases, current in circuit and voltage drop across the collector resistor R4 increases. The collector potential of transistor T5, and also the base of transistor T4 becomes more positive and further makes transistor T4 non-conducting. The internal resistance of transistor increases, current in the circuit and voltage drop across the emitter resistor of R2 decreases. The emitter potential of transistor T4, and also base of transistor T3 becomes more positive and further makes transistor T3 non-conducting. The internal resistance of transistor T3 increases, current in circuit and voltage drop across the emitter resistor R1 decreases. The emitter potential of transistor T3, and also the base of transistor T1 becomes more positive and further makes transistor T1 non-conducting. The internal resistance of transistor T1 increases, the emitter potential becomes more positive. As a result the voltage on the output decreases to the assigned magnitude -12V.

Capacitor C5, connected at output of the diagram of stabilized in parallel to working load, ensures the smoothing of the pulsation of the stabilized voltage with the short-term overloads.

II.4.4. Stabilized supply voltage -11,5V ÷ -13,56V (-U$_{SP}$).

The operation of the -U$_{SP}$ power supply without taking into account temperature dependence is analogous to the description of the operation of the -U$_N$ power supply of the arithmetic-logic unit.

Temperature fluctuations of the core memory unit lead to an appropriate change in the output voltage of the power supply.

A change in the output voltage occurs as a result the temperature dependence of the internal resistance of a thermistor. Thermistor Th in the diagram of the power supply is connected in parallel to the variable resistor R14 and is located in immediate proximity to the memory unit of the core store.

A temperature decrease causes an increase in the value of the resistance of thermistor and voltage divider of the base of transistor T8. The current in the circuit: 0V, R15, in parallel: R14, Th, D4, -U$_{SP}$, - and a voltage drop across the variable resistor R15 decreases. The potential of the base becomes more positive and further makes transistor T8 non-conducting.

Internal resistance of the transistor increases, and the collector of the transistor obtains a more negative potential, which through the first and second stages amplifier from transistors T7 and T6 enters the base of T2 and further opens transistor. The internal resistance of transistor decreases, the potential of the emitter becomes more negative. Voltage on the output of the power supply increases. An increase in the temperature causes the decrease of the value of the resistance of thermistor and voltage divider on the base of transistor T8. Current in the circuit: 0V, R15, in parallel: R14, Th, D4, $-U_{SP}$ - increases the voltage drop across variable resistor R15. The base potential becomes more negative and further opens transistor T8. The internal resistance of transistor T8 decreases. The collector of the transistor obtains a more positive potential, which through the first and second stage amplifiers enters the base and further makes transistor T2 non-conducting. The internal resistance of transistor T2 increases, and the emitter potential becomes more positive. Voltage on the output of the power supply decreases. Briefly the operation of the voltage regulating circuit is reduced to a change in the voltage on the output with a change of the resistance value in the voltage divider circuit, and the retention of the steady state voltage with the unchanging value of the bleeder resistance on the transistor base.

II.4.5. Stabilized supply voltage +12V ($+U_p$).

The source half-wave rectifier operates on the load with capacitive reaction. After switching on of the variable supply line voltage, in the transformer secondary winding S4 is induced an alternating voltage, which enters the anodes of diodes D10 and ZD1. Capacitor C2 of the smoothing filter is connected in parallel to resistor R22, Zener diode ZD1 and to the resistance of the working load. At the initial moment after the switching on of power unit, R22, Zener diode ZD1 and the resistance of the working load of the power supply are shunted by the discharged filter capacitor. The induced voltage in the secondary winding through the rectifier diode D10 creates a charge current in the capacitor. Capacitor C2 is charged, reactance X_C of the capacitor increases, current in the charge circuit decreases, voltage on the output of the power supply increases. The charge on capacitor C2 reaches almost to the amplitude value of the rectified voltage.

The secondary winding of the transformer is connected to resistor R22, Zener diode ZD1 and the resistance of working load. Half-wave current from the rectifier circuit on the secondary winding of the transformer flows only during one half-cycle, when forward voltage is connected to the rectifier diode. Let us assume that during the negative half-period diode D10 is connected to the forward voltage, in the circuit of the transformer secondary winding output 12, D10, R22, ZD1, output 13 of the transformer secondary winding, a current flows, which on the Zener diode ZD1 creates a voltage drop of 12V.

During a positive half-period diode D10 is connected the inverse voltage, which retains diode in the reversed biased state, in consequence of which current in the transformer secondary winding does not flow. Capacitor C2 begins to discharge. The discharge current does not change direction in the Zener diode chain and retains a voltage drop across ZD1 of 12V. Voltage on the capacitor plates decreases, but the sequential negative half-period from the secondary winding of the transformer recharges capacitor C2 through the forward biased diode D10, which in the negative half-period will again provide with the discharge current a corresponding voltage drop across Zener diode ZD1. The Zener diode cathode has positive potential with respect to the anode and is connected to the output of the power supply +12V. The anode is connected to the common 0V buss. A change in the value of the current flow within certain limits produces an appropriate change in the value of the internal resistance of Zener diode ZD1, which ensures a constant stabilized voltage on the output of the power supply +12V.

In parallel to the Zener diode ZD1 and to the resistance of working load is connected capacitor C3, which ensures the smoothing of the stabilized voltage for short-term overloads.

II.4.6. Un-stabilized supply voltage +100V (+Ua).

The power supply half-wave rectifier operates on the load with capacitive reaction. After switching on of the variable supply line voltage, in the secondary windings S1, S2 of the transformer an alternating voltage is induced, which enters the anode of diode D11 and resistor R30. The smoothing filter capacitor C10 is connected in parallel to resistor R26 and to the resistance of the working load. Operating conditions of the +100V and -90V sources occurs with the closing of contacts Lö2 of key Lö, which connects 0V to the winding of relay REL1. Relay REL1 operates and closes its contacts. Relay contact REL 1a is closed and connects the 0V (U_A) output of the +100V and -90V supplies through resistor R30 to output 10 of the transformer secondary windings S1.

Contact 1b of relay REL1 is closed and creates the latching circuit for the relay winding. At the initial moment after the switching on of the power supply, resistor R26 and the resistance of the working load of the power supply are shunted by the discharged filter capacitor. The induced voltage in the secondary windings of the transformer creates a charge current through the rectifier diode D11 and resistor R30 for capacitor C10. Capacitor C10 charges, reactance X_C of the capacitor increases, current in the charge circuit decreases, voltage on the output of the power supply grows. The charge of capacitor C10 reaches almost to the amplitude value of the rectified voltage.

The circuit of the transformer secondary winding is connected to resistor R26 and the working load resistance.

In the schematic of the half-wave rectifier the secondary current of transformer flows only during one half-period, when forward voltage is connected to the rectifier diode.

Let us assume that during the negative half-period the diode D11 is connected to forward voltage. In the circuit: output 7 of the transformer secondary winding S2, D11, parallel resistor R26, resistance of working load, resistor R30, output 10 of transformer secondary windings S1 - current flows. During the positive half-period, diode D11 is connected the inverse voltage, which ensures a reversed biased state of the diode. As a result of the diodes reversed biased state there is no current in the secondary windings of the transformer. Capacitor C10 begins to be discharged. Discharge current does not change direction in the load circuit. Voltage on the capacitor plates decreases, but in the sequential negative half-period the transformer secondary current through the forward biased diode D11 recharges capacitor C10.

II.4.7.   Un-stabilized supply voltage -90V (-U$_A$).

The source half-wave rectifier operates on the load with capacitive reaction. After switching on of the variable supply line voltage and pre-operation or relay REL1, in the transformer secondary winding S1 is induced an alternating voltage, which enters the cathode of diode D12 and resistor R30. Capacitor C11 of the smoothing filter is connected in parallel to resistor R23 and to the resistance of the working load. At the initial moment after the switching on of the power supply, resistor R23 and the resistance of the working load of the power source are shunted by the discharged filter capacitor. The induced voltage in the secondary winding of the transformer through the rectifier diode, resistor R30 and the closed contact of relay REL 1*a* creates a charge current in the capacitor circuit. Capacitor C11 is charged, the reactance X$_C$ of the capacitor increases, current in the charge circuit decreases, voltage on the output of the power source increases. The charge of capacitor C11 occurs almost to the amplitude value of the rectified voltage. The transformer secondary winding circuit is connected to resistor R23 and the resistance of the working load.

In the half-wave rectifier circuit transformer secondary current flows only in the time of one half-period, when forward voltage is connected to the rectifier diode. Let us assume that during the positive half-period diode D12 is connected to forward voltage. A current flows in the circuit: output 10 of the transformer secondary windings, R30, in parallel R23 and the resistance of working load, D12, output 9 of the transformer secondary windings S1. During the negative half-period diode D12 is connected to the inverse voltage and ensures its reversed biased state, as a result no current flows in the transformer secondary winding.

Capacitor C11 begins to discharge. The discharge current does not change direction in the load circuit. Voltage on the capacitor plates decreases, but current in the sequential positive half-cycle of the transformer secondary through diode D12 recharges capacitor C11.

II.4.8.   Operation of the power supply with a short circuit.

In the case of a short circuit in the load of the power supply voltage -U_N, on output -U_N of the power supply, -12V will be equal 0V, diode D1 is opened and connects emitter of transistor T5 to 0V of the source of autonomous power. Diode D5 is forward biased and connects the base of transistor T5 to the voltage divider formed from resistors R16, R29, R17.

A current begins to flow in the circuit: negative of the rectifier of source -U_N, R16, R29, D5, R7, R8. A voltage drop across resistors R7 and R8 creates a negative potential on the base and ensures the conducting state of transistor T5. Diode D3 is reverse biased. In the circuit: 0V, D1, emitter-base-collector of the conducting transistor, R4, R28, negative of the source of autonomous power - results in a current flow from the saturated operational condition of the transistor. The collector potential conducting transistor T5 becomes close to 0V. Transistor T4 is non-conducting. In the emitter circuit of the non-conducting transistor an insignificant current flows, the consequential voltage drop on resistor R2 can be disregarded. The emitter potential of transistor T4, and also the base of transistor T3, close to 0V, drives transistor T3 non-conducting. Similarly the emitter potential of transistor T3, and also the base of transistor T1, close to 0V, makes transistor T1 non-conducting. With a short circuit of the power supply the output -U_N enters a logic 0 signal and breaks the feed circuit for relay REL1.

The relay contacts are opened. Contact REL1 1a disconnects the secondary windings of the transformer from the -U_A and +U_A power sources. Contact REL 1*b* breaks the feed circuit of the relay, after the elimination of the short circuit transistor T1 will be in the conducting state, and relay REL1 will be in its initial state. Working voltage on the output of the power source will be restored after disconnection and re-closing of the mains supply voltage on the primary winding of the transformer. Operation of the -U_{sp} power source with a short circuit is analogous to the description of the operation of the -U_N power supply with a short circuit.

II.4.9.   Operational monitoring of the power supply
and installation of service voltages.

Checking and adjustment of the service voltages for the -U_N, -U_{sp}, +$U_p \pm U_A$ power supplies is carried out in the following order.

Voltage supply -12V (U_N):

1)   The potential switch of network to establish to 220V;

2) Connect the power unit through the regulation of the transformer core to the alternating current mains supply;
3) Connect a voltmeter between the $-U_N$ and $0b$ outputs of the power supply;
4) With the transformer voltage adjustment set the input voltage of the power unit to 220V;
5) With variable resistor R7 adjust the output of the $-U_N$ voltage source to -12V;
6) By sequential switching of the transformer voltage adjustment vary the input voltage of the power unit by $220^{+10\%}_{-10\%}$ V. With a proportional change on the input voltage the fluctuation of the $-U_N$ output voltage must be $-12 \pm 5\%$ V;
7) Operational noise conditions of the supply must not exceed 15mV.

Voltage supply $-11,5 \div -13,66V$ ($-U_{sp}$):

1) The potential switch of network to establish to 220V;
2) Connect the power unit through the regulation of the transformer core to the alternating current mains supply;
3) Connect a voltmeter between the $-U_{sp}$ and $0b_{sp}$ outputs of the power supply;
4) Unsolder one end of thermistor and connect consecutively to its connecting points two decade resistors (0, 1, 2, 3 … 10 X by 1000R and 0, 1, 2, 3… 10 X by 100R). The value of the resistance of thermistor at 15 and $40^{\circ C}$ temperatures is indicated in the table, fastened to the power unit;
5) With the transformer voltage adjustment set the input voltage of the power unit to 220V;
6) Establish with decade resistors the value of thermistor at 15 $^{\circ}$C;
7) Adjust variable resistor R14 to obtain -13,5V on the output of the -Usp source;
8) Establish with decade resistors the value of thermistor at 40 $^{\circ}$C;
9) Adjust variable resistor R15 to obtain -11,5V on the output of the -Usp source;
10) Establish with decade resistors the value of thermistor at 15 $^{\circ}$C and verify the voltage on the -Usp output which must be $-13 \pm 5\%$ v. With any deviation from the permissible limits adjust variable resistor R14 to obtain -13,5V on the output of the -Usp source;
11) Establish with decade resistors the value of thermistor at 40 $^{\circ}$C and verify the voltage on output -Usp which must be in the limits $-11,5 \pm 5\%$ V. With any deviation from the permissible limits adjust variable resistor R15 to obtain -11,5V on the output of the -Usp source;
12) Repeat point 10 installing decade resistors and measure the voltage on the output of source -Usp, which must satisfy the requirements of point 10. With any deviation from the permissible limits adjust variable resistor R14 to obtain -13,5V on the output of the -Usp source;

13) Repeat point 11 installing decade resistors and measure the voltage on the output of source -Usp, which must satisfy the requirements of point 11. With any deviation from the permissible limits adjust variable resistor R15 to obtain -11,5V on the output of the -Usp source,

14) Switching decade resistors and adjustment in the sequence of points 12 and 13 is carried out before obtaining on the output of source -Usp of operating voltage within the limits, indicated in points 10 and 11;

15) Establish with decade resistors the value of thermistor at 15 $^{\circ}$C;

16) By sequential switching of the transformer voltage adjustment vary the input voltage of the power unit by $220^{+10\%}_{-10\%}$ V. With a proportional change on the input voltage the fluctuation of the -Usp output must not exceed the permissible limits of point 10;

17) Establish with decade resistors the value of thermistor at 40°C;

18) Repeat test point 16. The fluctuation of voltage on the output of source -Usp must not exceed the permissible limits, indicated in point 11;

19) Operational noise conditions of the supply must not exceed 15mV.

Voltage supply +12V (+Up):

1) The potential switch of network to establish to 220V;

2) Connect the power unit through the regulating transformer core to the alternating current mains supply;

3) Connect a voltmeter between the +Up and 0*b* outputs of the power supply;

4) With the transformer voltage adjustment set the input voltage of the power unit to 187V. Voltage on the output of the +Up supply must be ≥ to 10,8V;

5) With the transformer voltage adjustment set the input voltage of the power unit to 242V. Voltage on the output of the +Up supply must be ≤ to 13,2V;

6) Operational noise conditions of the supply must not exceed 0,3 mV.

Voltage supply +U$_A$, U$_A$.

1) The potential switch of network to establish to 220V;

2) Connect power unit through the regulating transformer core to the alternating current mains supply;

3) Connect a voltmeter between the +U$_A$ and U$_A$ outputs, and a second voltmeter between the U$_A$ and U$_A$ outputs;

4) Press the Lō key to create an electrical feed circuit through relay REL1;

5) With the transformer voltage adjustment set the input voltage of the power unit to 187V. Voltage on the +U_A output must be ≥ +76V. Voltage on the -U_A output must be ≤ -82V;

6) With the transformer voltage adjustment set the input voltage of the power unit to 242V. Voltage on the +U_A output must be ≥ +100V. Voltage on the -U_A output must be ≤ -108V;

7) Voltage on outputs -U_A +U_A should be regulated by the appropriate switching of the secondary winding S2 of transformer.

Voltage supply ~ 110 VG:

1) To establish the potential switch of network on 240V;
2) To connect power unit through the regulating transformer core to the alternating current mains supply;
3) Connect a voltmeter between the 1V2 and 2V2 outputs;
4) To establish by regulating transformer voltage on the input of the power unit of 240V. Voltage on the output of the source of ~110V in must be near 110V.

II, 4.10. Component values of the power supply.

Transistors

T1	2SB228	
T2	2SB80-1	
	(2SB368-1)	β=29÷55
T3	2SB80-1	
	(2SB367-1)	
T4	SA25/2	β=72÷55
T5	SA25/4	
T6	2SB80-1	
	(2SB368-1)	β=29÷55
T7	SA25/2	
T8	SA25/4	β=72÷166

Electrolytic Capacitors

C1	5000uF	25V
C2	500uF	25V
C3	500uF	25V
C4	500uF	25V
C5	1000uF	15V
C6	1000uF	15V
C9	5uF	30V
C10	100uF	150V
C11	100uF	150V
C12	2uF	50V
C14	10uF	25V

Germanium Diodes

D1	OA741
D2	OA741
D3	Gu100
D4	Gu100
D5	1N35 (GAZ17)
D6	1N35 (GAZ17)
D7	Gu100
D8	Gu122
D9	Gu122
D10	Gu112
D11	Gu103
D12	Gu103

Silicon diodes

| ZD1 | SZ512 | (ZL12) |
| ZD2 | SZ506 | (ZL6,8) |

Resistors

R1	1K	0.25W	10%
R2	2K7	0.125W	10%
R3	390R	0.05W	10%
R4	2K7	0.125W	10%
R6	560R	0.125W	10%
R7	P 1K		
R8	1K2	0.125W	10%
R9	1K	0.25W	10%
R10	5K6	0.05W	10%
R11	2K7	0.125W	2%
R12	1K2	0.125W	10%

Paper Capacitors

| C7 | 0.1uF | 63V |
| C8 | 0.22uF | 63V |

Resistors

R13	220R	0.25W	10%		R27	1K	0.125W	10%
R14	P 25K				R28	100R	0.05W	10%
R15	P 10K				R29	1K5	0.05W	5%
R16	3K3	0.125W	10%		R30	33R	0.5W	10%
R17	1K5	0.125W	10%					
R20	200R	0.05W	10%		**Relay**			
R21	1K	0.125W	10%		REL1 GBR312-12			
R22	33R	0.25W	10%					
R23	10K	2W	10%		**Anti- Interference filter**			
R26	10K	2W	10%		D0,1 +2500/B/200 V 10%			

Line voltage and earthing are connected to the power unit through connector V1

Connector V1

Power unit	Contact number	Line voltage
1V2	1	220V (a)
Safety device	2	220V (b)
Machine frame	3	Boot-tree of supply lead from the network and the grounding

Working voltages of the power supply are connected to the arithmetic-logic unit through connector V2.

Connector V2

Location of power supply connector contacts		Signals and voltages	Location of arithmetic-logic unit connector contacts		
1V1	1	220V (a)	1		3V3
5Tr1	2	110 VG	2		30V6
Interference suppression capacitor	3	220V (a) RWN	3		30V6
	4	220V (a) RWN	4		1V3
D11; C10; R26	5	$+U_A$	5		1V3
	6		6		
D12; C9, 11; R23, 26	7	$-U_A$	7	11/12	
REL 1a; C10, 11; R23, 26	8	U_{A0}	8	2/11	
T2; D2, 4; C6	9	$-U_{SP}$	9	20/1	
	10	$-U_{SP}$	10	20/1	
14Tr1; REL 1b; ZD1, 2	11	0_V	11	60/3	
C1, 2, 3, 4, 5, 6, 7, 8, 12, 14; R1, 2, 8, 9, 10, 15, 17, 21;					
Ov_{sp}	12	0_V	12	60/2	8V5
ZD1; C3; R22	13	$+U_P$	13	61/1	
T1;11Tr1; REL1; D1, 3;	14	$-U_N$	14	62/1	
C4, 5, 9; R12, 20, 27	15	$-U_N$	15	62/2	
REL1; REL 1b	16	PEL1	16		13V3
	17		17		
	18		18		14V3
0V	19	$0V_{sp}$	19		15V3
	20	$0V_{sp}$	20		16V3

II.5.   Keyboard input unit.

Entering digital information, display, initialisation of the arithmetic-logic unit into its initial state, commands for the completion of arithmetic operations, record, erasure and re-writing of information in the memory registers are all carried out by the keyboard input unit.

The necessary information from the input unit enters the arithmetic-logic unit in a specific sequence, which accomplishes the corresponding operations.

Connections V3 and V4 create the overall electrical circuit of the arithmetic-logic unit and information input. All the necessary operating voltages of the power supplies are supplied to the keyboard input unit via connector V3 from the arithmetic-logic unit.

Connector V3

Location of input unit connector contacts		Signals and voltages	Location of arithmetic-logic unit connector contacts	
The double-throw contact of power switch AUS-EIN	1	220V (a) RWN	1	4V2
	2		2	
Dead contact of power switch AUS-EIN	3	220V (a)	3	1V2
	4		4	
Double-throw contact "* I"	5	0V	5	60/1
Dead contact Lö 2	6	0V	6	
Closed contact =	7	K	7	30/9
	8		8	
	9		9	
	10		10	
	11		11	
Double-throw contact 2Lö	13	PEL1	13	16V2
Double-throw contact 1,3; Lö	14	$0V_{sp}$	14	18V2
	15	$0V_{sp}$	15	19V2
	16	$0V_{sp}$	16	20V2
Closed contact 1; Lö	17	$0V_{sp}A$	17	37/1
	18	$0V_{sp}A$	18	38/1
	19	$0V_{sp}A$	19	39/1
Dead contact #	20	#K	20	24/11

Connector V4 connects the digital and functional keyboard to the diode encoders of the arithmetic-logic unit logic 0 signals during switching of the corresponding contacts of the keyboard input unit.

Connector V4

Location of input unit connector contacts		Signals		Location of arithmetic-logic unit connector contacts	
Dead contact of key	"1"	1	1k	1	54/12
	"2"	2	2k	2	53/12
	"3"	3	3k	3	52/12
	"4"	4	4k	4	51/12
	"5"	5	5k	5	50/12
	"6"	6	6k	6	48/12
	"7"	7	7k	7	47/12
	"8"	8	8k	8	46/12
	"9"	9	9k	9	45/12
	"10"	10	0k	10	55/12
	"11"	11	,k	11	43/12
	"12"	12	+k	12	22/12
	"13"	13	-k	13	21/11
	"14"	14	xk	14	41/11
	"15"	15	:k	15	30/11
	"16"	16	$x^n k$	16	35/11
	"17"	17	=k	17	42/11
	"18"	18	Ck	18	44/12
	"19"	19	+ Ik	19	27/11
	"20"	20	+ IIk	20	17/11
	"21"	21	+ IIIk	21	19/11
	"22"	22	- Ik	22	33/11
	"23"	23	- IIk	23	34/11
	"24"	24	- IIIk	24	26/11
	"25"	25	* Ik	25	38/11
	"26"	26	* IIk	26	37/11
	"27"	27	* IIIk	27	25/11
	"28"	28	k	28	36/11
	"29"	29	k	29	40/11
	"30"	30	k	30	31/11
	"31"	31	Lö	31	52/7
	"32"	32	Lösp	32	11/1

When not in use a logic 0 signal from keyboard unit inputs the arithmetic-logic unit through connector contacts 5,6V3, the serially connected contacts of the keyboard and connector contact 7V3 inputs to the circuit diagram (Fig. 19). From the circuit diagram output a logic 0 signal enters the equivalent components of the arithmetic-logic unit schematic and ensures the assigned operating mode.

In the initial state of the keyboard switch contacts the logic 0 signal does not input the diode encoders.
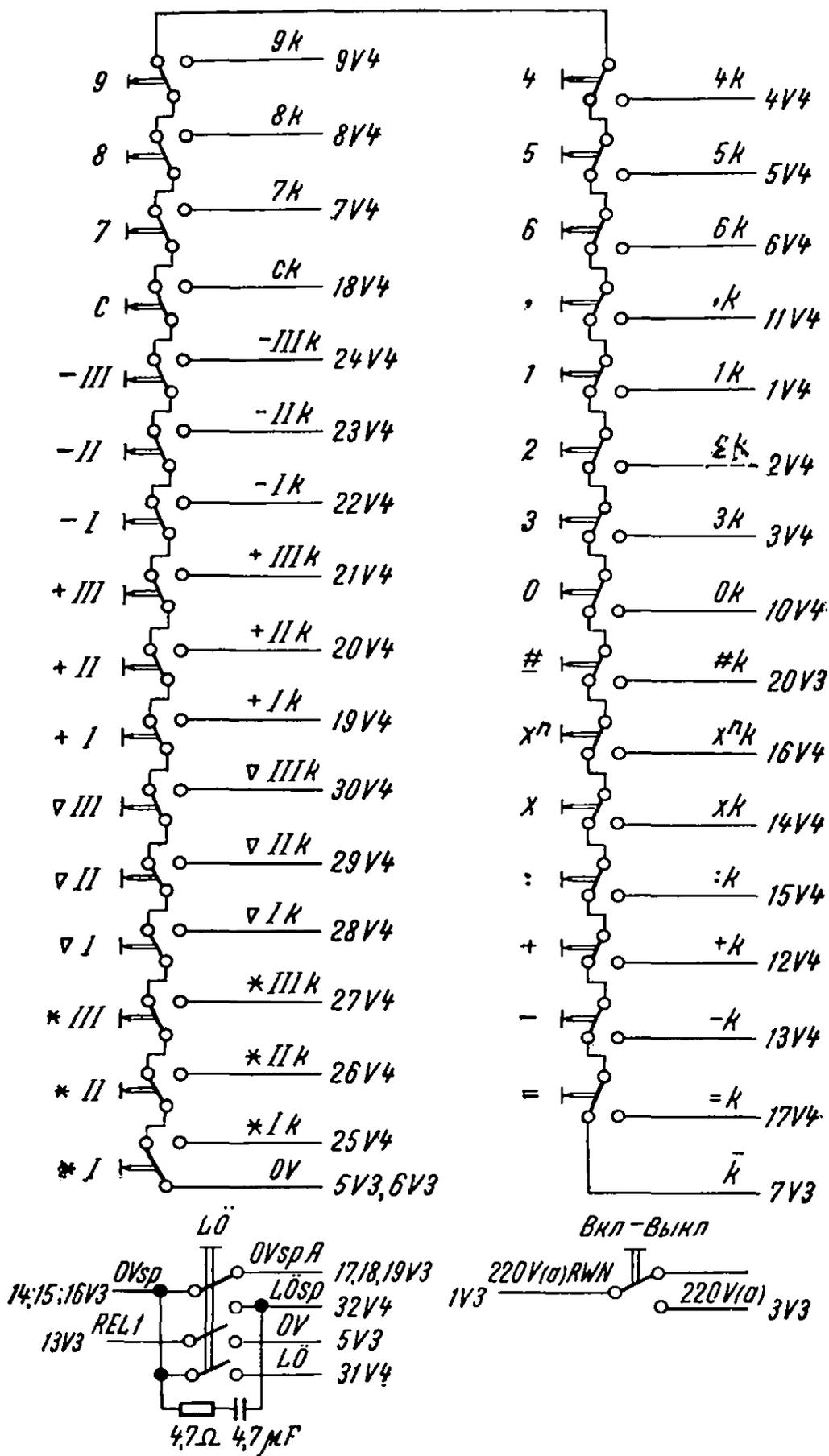
Fig. 19. Keyboard Input unit circuit diagram.

As a result of this at outputs of the digital and functional keyboard encoder schematics a logic 1 signal is generated.

In the process of entering information, operation of a switch contact leads to switching of a logic 0 signal from input K to one of the inputs of the encoder of digital or functional keyboard.
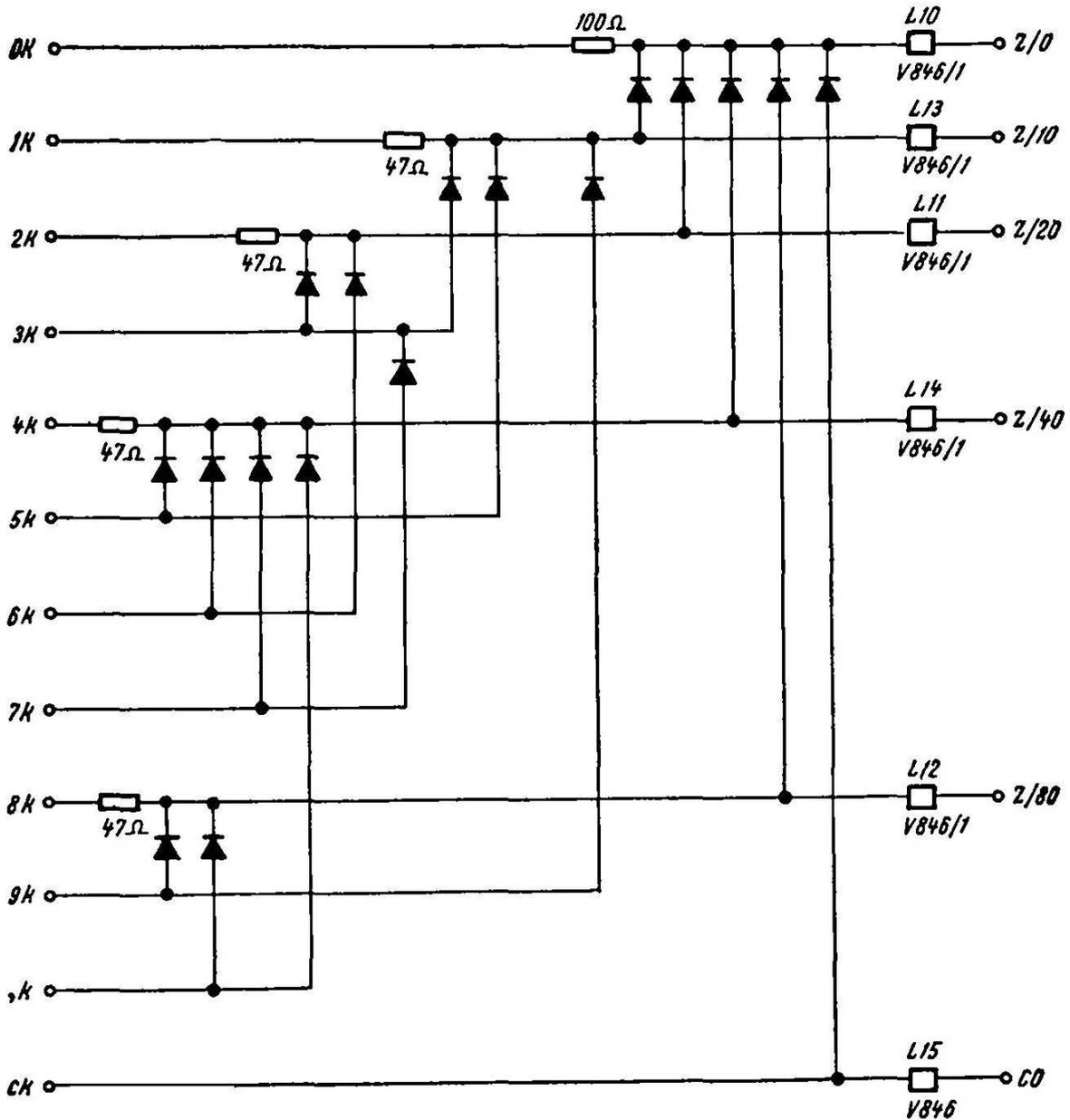
Fig. 20, Electrical schematic the digital keyboard encoder.

The encoder diodes ensure the connection of the logic 0 signal to the inputs of the corresponding connection diagrams. Consequently, after the connection of a logic 0 signal at outputs of the circuit diagrams a logic 0 output signal is generated. After turning off the logic 0 signal from input K at output to the overall keyboard connection diagram a logic 1 signal is generated equal to the time the switched contact has been pressed.

Fig. 21. Schematic circuit diagram of the keyboard function encoder.
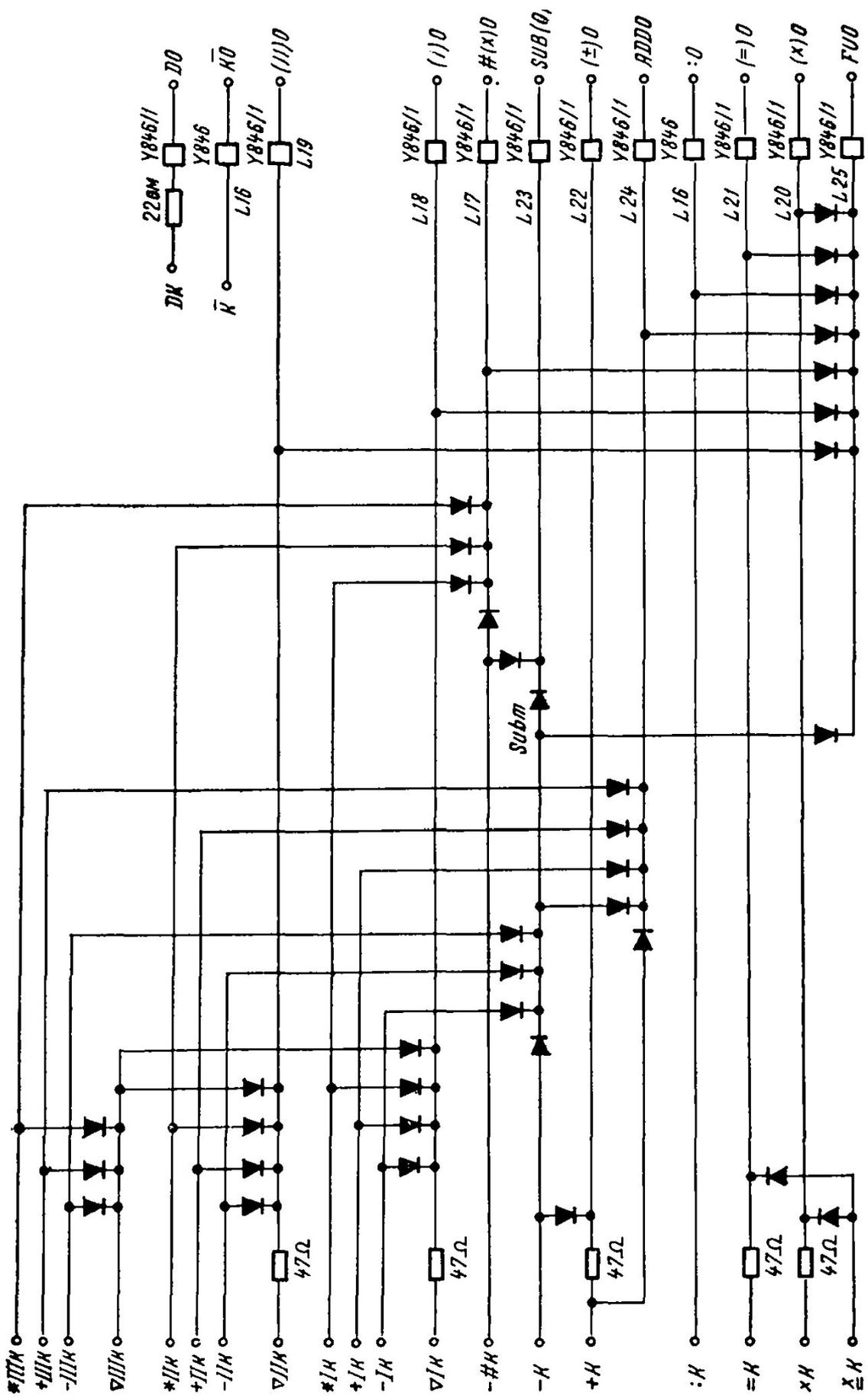
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The decimal digital keyboard encoder ensures the encoding of the number keys into the Binary Coded Decimal numeration system.

Example, let us examine the operation of the digital keyboard encoder based pressing the number 3 key.

After switching the contact for the "3" key to input 3k of the diagram a logic 0 signal is connected, which through the diodes enters the inputs of the filter circuits of L11, L13, L10. At outputs Z/0, Z/10, Z/20 of the filter circuits a logic 0 signal is generated, and at the outputs Z/40, Z/80, C0 of the remaining encoder connection diagrams – logic 1 signals.

The signals of all digital keys, key for the decimal point key and for the correction key "C" are coded by the encoder diodes and by the filter circuits as logic 0 and 1 signals in accordance with the following table:

Swit-ched key	Encoder output											
	1	2	3	4	5	6	7	8	9	0	,	C
Z/0	0	0	0	0	0	0	0	0	0	0	0	0
Z/10	1	1	0	1	0	1	0	1	0	1	1	1
Z/20	1	1	0	1	1	0	0	1	1	1	1	1
Z/40	1	1	1	0	1	0	0	1	1	1	0	1
Z/80	1	1	1	1	1	1	1	0	0	1	0	1
C0	1	1	1	1	1	1	1	1	1	1	1	0

Devices and operation of the functional keyboard encoder (Fig. 21) are similar to the description of the digital keyboard encoder.

II.6.   Decimal point selection switch.

The decimal point position switch consists of four switch wafers, each of which has 12 fixed positions. Different positions of the switch ensure the appropriate display of the decimal point, and the combination of word length of the entered digital information with arithmetic operations into the memory unit registers. The quantity of numerical decimal digits after the decimal point or the degree of accuracy of calculations is determined by the position of the decimal point switch. Setting the decimal point switch is effected by a numbered disk, which has the designations - 0, 1, 2, 3, 4, 6, Z, 9, 10, 11, 12, 14, which on the schematic circuit diagram (Fig. 22) corresponds to the position of the contact of wafer E4 and to outputs L1, L2, L3, L4, L6, L9, L10, L11, L12, L14.

Connector V5 connects the decimal point position switch circuit with the arithmetic-logic unit into the overall machine electrical diagram. 0V through the connector pin 8V5 from the arithmetic-logic unit enters the sliding contacts of all four switch wafers. Depending on the position of the decimal point position switch a logic 0 signal passes through the appropriate outputs and pins of connector V5 to the specific component parts of the arithmetic-logic unit.

Fig. 22. Circuit diagram of the Decimal Point position switch.

Connector V5

Location of decimal point switch connector contacts		Signal designation	Location of arithmetic-logic unit connector contacts	
Contacts 3, 5, 6 of wafer 2; " 1 of wafer 3	1	G11	1	10/10
" 10, 11, 12 of wafer 2	2	G14	2	39/10
" 8, 9, 10, 11, 12 of wafer 3	3	G18	2	18/10
" 2, 4 of wafer 2	4	G21	4	47/10
" 2, 3, 6 of wafer 1	5	G22	5	8/10
" 8, 9, 10, 11 of wafer 1	6	G24	6	1/10
" 2, 3, 4, 5, 6 of wafer 3	7	G28	7	2/10
Common contact of wafer 1, 2, 3, 4	8	0V	8	12V2
Contacts 4, 5, 12 of wafer 1; " 8, 9 of wafer 2	9	DiV 01k	9	21/9
	10			
	11			

Simultaneously in accordance with the position of the decimal point switch a logic 0 signal through one of the contacts of connector V9 is connected to the display and ensures the illumination of one of the appropriate decimal point lamps.

The second contact of all the lamps of the decimal point display are connected through a resistor of 270 ohms of 0,25w and contact of 29V6 to the power supply -U_N (fig, 26).

Connector V9

Location of decimal point switch connector contacts		Signal designation	Location of arithmetic-logic unit connector contacts		
Contact 2 of wafer 4	1	L1	1	Dp lamp	1
Contact 3 of wafer 4	2	L2	2	Dp lamp	2
Contact 4 of wafer 4	3	L3	2	Dp lamp	3
Contact 5 of wafer 4	4	L4	4	Dp lamp	4
Contact 6 of wafer 4	5	L6	5	Dp lamp	6
Contact 8 of wafer 4	6	L9	6	Dp lamp	9
Contact 9 of wafer 4	7	L10	7	Dp lamp	10
Contact 10 of wafer 4	8	L11	8	Dp lamp	11
Contact 11 of wafer 4	9	L12	9	Dp lamp	12
Contact 12 of wafer 4	10	L14	10	Dp lamp	14
	11				

II.7. Memory unit.

The memory unit consists of toroidal ferrite cores, assembled into digital matrices.

Ferrite cores are manufactured from a ceramic ferromagnetic material, whose general formula is $MO \cdot F_2O_3$, where M is one of the bivalent metals. Note - Iron oxide is Fe_2O_3.

The characteristic properties of ferromagnetic materials can be attributed the following properties, which are used and are considered in the memory units from the ferrite cores:

1) The materials internal magnetic field can considerably exceed its induced magnetic field H;

2) Remnant induction Br remains for a long time without the expenditure of additional energy;

3) The ferromagnetic properties of the material varies with an inverse temperature dependence. For each material there is its critical temperature point, which when exceeded leads to the loss of the ferromagnetic properties of the material.

In storage cores the remnant induction Br is created as a result the action of a magnetic field by the tension Hm, which is formed by the passage of a current of a specific value, equal to I_m, through the ferrite cores winding.

Depending on the current direction I_m and the corresponding magnetic field the remnant induction of a ferrite core is characterized as the state of +Br or -Br.

Different states of remnant induction determine the two steady states of a ferrite core, which in the memory unit are used for storage of information, which has values of 0 and 1.
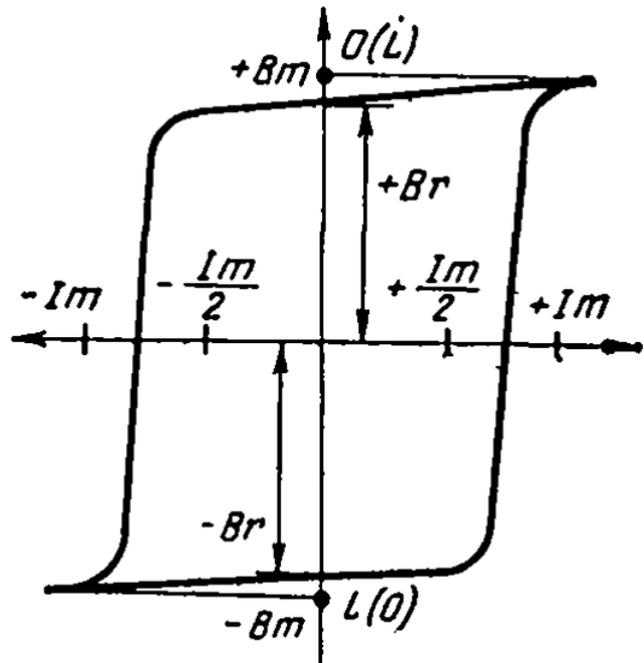

Fig. 23. Ferrite core hysteresis loop.

The polarity reversal of a ferrite core and the corresponding change in the remnant induction ±Br is ensured as a result the action of a magnetic field by the tension Hm.

The value of the magnetic field depends on the direction and value of current I_m, taking place through the ferrite cores winding. The curve of a change in the magnetic induction of the sequential reversal of polarity of ferrite core is called an hysteresis loop (Fig. 23).

The principle of the operation of a ferrite core storage unit is based on the coincidence of the half-current $\dfrac{Im}{2}$ in the corresponding wires, which fulfils the function of a single-turn winding of a ferrite core.

II.7.1. Reading information from a ferrite core.

The ferrite core has 2 sensing wires of discharge of one direction and ensure the readout of the information of core only when $\dfrac{Im}{2}$ current pulses are synchronised (Fig. 24).

Each half-current creates a magnetic field by the tension $\dfrac{Hm}{2}$.

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The resulting magnetic field of two half-currents $\dfrac{Hm}{2} + \dfrac{Hm}{2} = Hm$ produces the polarity reversal of a ferrite core. Let us assume that the information 0 corresponds to the remnant induction of +Br. Information 1 corresponds to remnant induction -Br. A change in the magnetic induction from -Br to +Bm directs an EMF of a corresponding amplitude onto the read wire. The information 1 signal passes through the read amplifier and enters the arithmetic-logic unit of the machine.
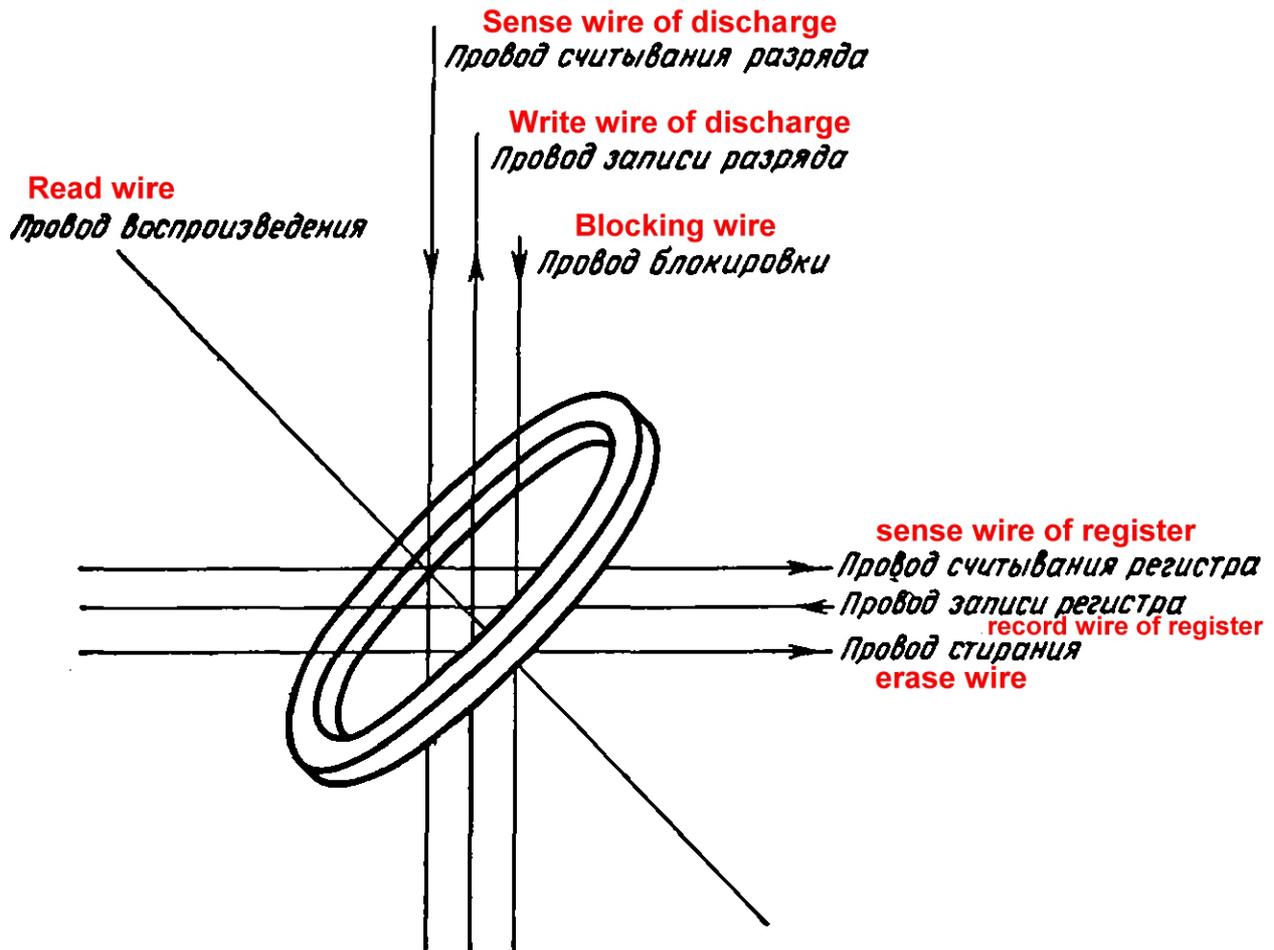

Fig. 24. Diagrammatic representation of a ferrite core.

Information 0, written on the ferrite core, is read by the resulting magnetic field HM without the reversal of polarity of core, since a change in the magnetic induction varies from +Br to +Bm, and produces an EMF on the read wire, which corresponds to the amplitude of counted information 0. After the end of a read pulse the magnetic induction of a core varies from +Bm to +Br, as a result of which on the read wire it is directed interference.

The amplitude of counted information 0 is equal to the amplitude of interference, but it is of a reversed phase. The current pulses $\dfrac{Im}{2}$, which do not coincide in time, do not provide a sufficient tension of magnetic field, which does not cause the reversal of polarity of ferrite core.

II.7.2. Writing information to a ferrite core.

Current pulses $\frac{Im}{2}$ on the write wires register synchronize and direction. The resulting magnetic field can equal Hm only when through the blocking (inhibit) wire it does not flow an opposing current $\frac{Im}{2}$. The polarity reversal of a core for writing occurs analogously with the reading of information, with the difference that EMF, induced by a change of inducting the ferrite core from +Br to -Bm, on the read wire does not produce a useful signal (fig, 24). After the end of a write pulse the magnetic induction of core varies from -Bm to -Br. As a result interference is produced on the read wire.

The erasure of the written information is ensured by a logic 1 level current pulse, which flows in the erase wire only with the start of the corresponding keys. In the memory unit each matrix is divided into 6 registers of 16 digits and ensures a storage of 96 bits. Consequently, four matrices create 6 registers in groups of four ferrite cores of 16 digits.

The planes of ferrite cores for digits 1 through 15 are used for storing digital information in the binary coded decimal numeration system. The group for the 16th digit is used for storing the sign of a number. Positive sign is depicted as code zero 0000; the sign "minus" - by the code of one 0001.

Memory unit registers according to the functions carried out are divided into operational registers MD, MR, AC0 and accumulating registers AC1, AC2 and AC3.

The binary coded decimal of any decimal digit is consecutively formed at output of the encoder in proportion to the decimal number entered on the keyboard input unit. The arithmetic-logic unit ensures writing of the entered digital information into the groups of corresponding digits of the MR register.

The code of sign "minus" corresponds to the record of one 0001.

The writing of digital information and sign of the number into the other registers is ensured by the arithmetic-logic unit via rewriting from register MR by the pressing of the corresponding functional keys.

The memory unit is located in the arithmetic-logic PCB unit and is internally connected with it.

II.7.3. Logic symbols of the memory unit connections.

The first and second numbers indicate the location of the corresponding connection with the lower or upper PCB assembly of the memory unit (01 - lower PCB, 02 - upper PCB).

The third and fourth numbers indicate, on what side of the PCB assembly is located the corresponding connection (Fig. 25).

Beginning from the mitred corner, the sides are designated **anti-**clockwise by numbers 01, 02, 03 and 04, if we look in the direction of the wires of the corresponding PCB. The fifth and sixth numbers indicate the number of each joint. The connections of each side have numbers from 01 to 23 or from 01 to 21.
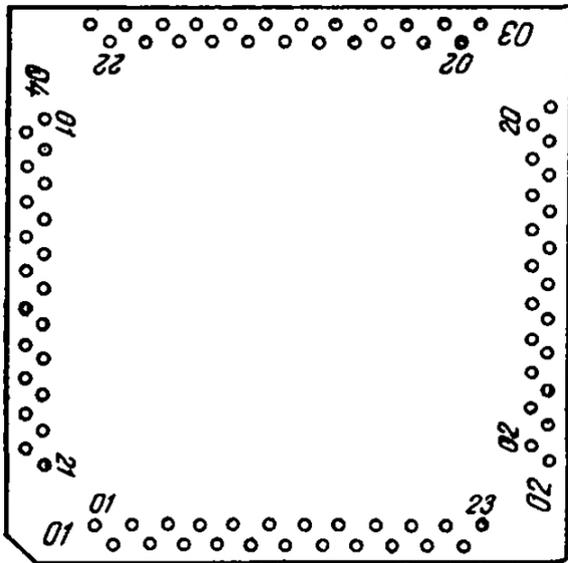

Fig. 25. The common form of assembly of a memory unit.

II.8. Display unit.

The display unit consists of 15 digital lamps, which ensure the visual delivery of the entered digital information, results of arithmetic operations and calculations.

Each digital lamp is a glow discharge device, which has one anode and ten numerical cathodes from 0 to 9. Connector V6 connects the display unit circuit with the arithmetic-logic unit into the overall electrical diagram. The signals of the operating voltage $+U_A$ are consecutively generated at outputs $S1 \div S15$ of the display anode driver amplifiers. From the output of the anode amplifiers consecutive $+U_A$ signals are connected through contacts $12 \div 26$ of connector V6 to the anodes of the digital lamps $RO1 \div RO15$ (Fig. 26).

The signals of operating voltage $-U_A$ are generated at outputs $0 \div 9$ of the display cathode driver amplifiers. From the output of the signal amplifiers voltage $-U_A$ are simultaneously connected through contacts $1 \div 10$ of connector V6 to the appropriate numerical cathodes of the display lamps $RO1 \div RO15$. The illumination of the number cathode of the indicator light, which corresponds to the byte of memory unit, occurs when the anode and the cathode simultaneously through the contacts of connector V6 reaches the ignition voltage, equal to a potential difference of $+U_A$ and $-U_A$. The synchronization of the $+U_A$ and $-U_A$ signals is created by the operation of the arithmetic-logic unit.

The display of digital information from the memory unit occurs only from the ferrite cores of the MR register. The display of the digital information of the remaining registers occurs as a result of re-writing information into the MR register after pressing the corresponding functional keys.

11 miniature incandescent lamps placed in the display show the position of the decimal point, the "minus" sign is located on the right side of the display block above the neon lamp that indicates a supply of line voltage.
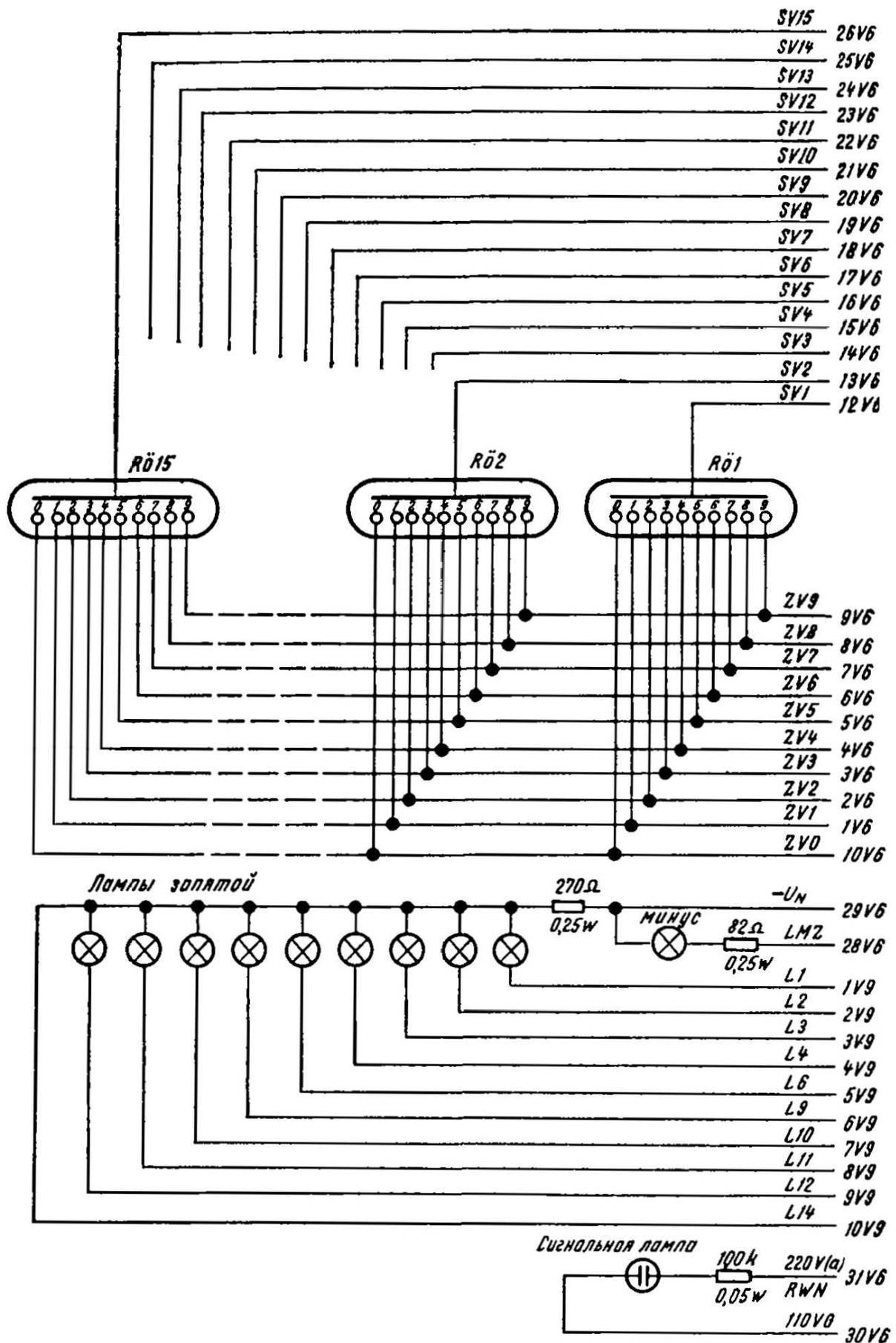
Fig. 26. Schematic Circuit diagram of the display unit.

Connector V6

Location of display unit connector contacts			Signal designation	Location of arithmetic-logic unit connector contacts	
Cathode	1	1	ZV1	1	38/12
"	2	2	ZV2	2	32/12
"	3	3	ZV3	3	8/12
"	4	4	ZV4	4	20/12
"	5	5	ZV5	5	24/12
"	6	6	ZV6	6	17/12
"	7	7	ZV7	7	7/12
"	8	8	ZV8	8	15/12
"	9	9	ZV9	9	9/12
"	10	10	ZV0	10	36/12
		11		11	
Lamp anode	1	12	SV1	12	4/11
" "	2	13	SV2	13	5/11
" "	3	14	SV3	14	6/11
" "	4	15	SV4	15	7/11
" "	5	16	SV5	16	8/11
" "	6	17	SV6	17	9/11
" "	7	18	SV7	18	10/11
" "	8	19	SV8	19	12/11
" "	9	20	SV9	20	13/11
" "	10	21	SV10	21	15/11
" "	11	22	SV11	22	16/11
" "	12	23	SV12	23	55/11
" "	13	24	SV13	24	56/11
" "	14	25	SV14	25	57/11
" "	15	26	SV15	26	58/11
		27		27	
82R 0.25W		28	LMZ	28	12/8
270R 0.25W		29	$-U_N$	29	62/3
Line voltage indication		30	110VG	30	2V2
0.1R 0.05W		31	220V (a)RWN	31	3V2
		32		32	

Signal name table for the functional diagrams

SCHREIB	-	Write	MUL	-	Multiplication
LES	-	Read	DIV	-	Division
EING	-	Input	ÜBER	-	Transfer
Lō	-	Erase	VOR	-	Preparation
ADD	-	Addition	RU	-	Conversely
SUB	-	Subtraction	VER	-	Shift

Chapter III

Functional operation of the calculation machine.

In the description of the operation of the machines functional diagram some reductions in the description of the operational sequence of the component parts have been made, the following expressions serve as an example of a reduction:

1) "From output A of gate K… a positive voltage drop sets flip-flop into the working condition". Description of the operation of the component parts without the reduction; "A change in the logic 1 or 0 signal at output A of the diagram leads to capacitor discharge of the differentiating circuit. At output A of the differentiating circuit a positive polarity pulse is generated, which enters input B1 and sets the flip-flop into the working condition".

2) "Clock pulse S through gate K… resets flip-flop F into the initial state".
In this case the sequence of the diagram operation occurs in the following order: "*Clock pulse S enters input K of the gate… at the output of the gate a negative polarity pulse is generated, which is fed to the input of the differentiating circuit and in the sequence of describing point 1 ensures the inversion of the flip-flops*". Analogous reductions in the text are allowed for the purpose of compactness in the operational account of the machine functional diagram.

I11.1. Operating conditions of the machine schematic and control of read and write cycles.

Preparation of the machine for arithmetic operations is effected by the turning the EIN - AUS (ON-OFF) switch disk to the operating position, the position ensures the closing of the switch contacts (Fig. 19) the joint of 1V3, 3V3 and the connection to the mains supply voltage of the primary windings P1, P2, P3, P4 of the transformer (Fig. 18).

The current, flowing in the primary windings, induces an EMF on the secondary windings S1, S2, S3, S4, S5, S6 of the transformer ensuring the necessary voltages are present at the power supply unit outputs.

Closing and switching the corresponding contacts of the Lö key carries out the following series connection (Fig. 19), which completes the functions.

1. The switched contact Lö1 through the connection diagram u846 connects 0V, to the circuit (Fig. 27) and ensures the erasure of the memory unit operational registers with a current pulse of Im from the charge of a 20uF capacitor through a resistor of 15 ohms.

2. The closed contact Lö2 connects 0V to and creates the electrical energizing circuit of relay REL1 (Fig. 18):

a) The contact of the relay REL1a connects voltage U_{A0} to output connection 8V2 of the power unit;

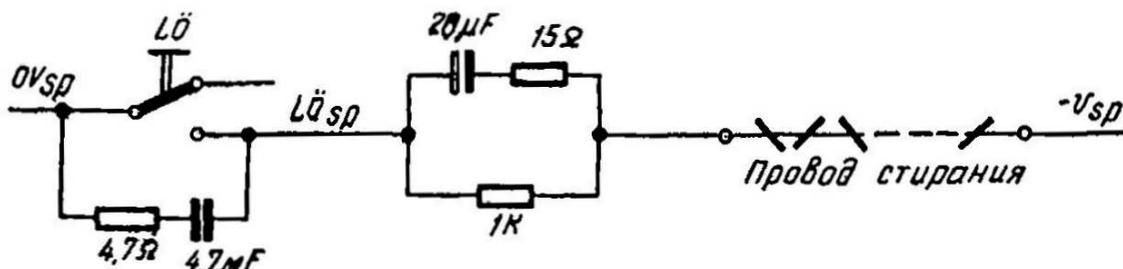b) The contact of relay REL1a creates a latching circuit for relay REL1.

Fig. 27.   Schematic circuit diagram of operational register erasure.

3. The closed contact Lö3 connects $0V_{sp}$ to the collector inputs of the appropriate flip-flops of the arithmetic-logic unit into their initial state, resetting them.

After switching on the power unit the voltage $-U_N$ ensures the starting of multivibrator M, whose pulses enter the input of inverter N37. At output of the inverter inverted clock pulses S with a frequency of 25Khz are generated. Pulses S have a negative polarity and form a close to rectangular signal.

Principally the reading and writing of information in the registers of the memory unit depend on the functions carried out and occurs consecutively, beginning from the four bits of the specific byte, control of the display operation is provided by the flip-flops of the Z counter through the appropriate logical AND gates.

Operational control of registers is carried out by logical "AND" and "OR" gates.

I
II.1.1.   Incremental counting of the Z counter.

Starting the Z counter occurs as a result of the setting of one or several flip-flops depending on the requirements of operational control by the bytes of the memory unit.

In the initial state of the Z counter, which consists of flip-flops Z1, Z2, Z4, Z8 and Z16, from outputs Z1, Z2, Z4, Z8 inverters N79, N81, N83, N84 and from the output of flip-flop Z16 to the inputs of gate D13 logic 0 signals are entered. From the output of gate D13 a logic 0 level signal enters inverter N36.

The phase of the input signal is inverted from output $\overline{Z}$ of inverter N36, a logic 1 signal enters the inputs of the corresponding functional diagrams, including input $\overline{Z}$ of gate K66. Let us assume flip-flop S1 is reset, from output $\overline{S1}$ a logic 1 signal is fed to the input of inverter N30. The phase of the input signal is inverted, so from output S1 of the inverter a logic 0 signal enters the control input E2 of the differentiating circuit of its flip-flop. A clock pulse S with a negative voltage drop disables, and with positive enables gate K66. At the output of the gate a pulse is generated of identical polarity and close in their parameters to the clock pulse S, which enters input E1 of the differentiating circuit of flip-flop S1. At output A of the differentiating circuit is generated a peak positive polarity pulse, which enters input B1 of flip-flop S1 and sets it. As a result from output $\overline{S1}$ of the flip-flop a logic 0 signal is fed to the input of inverter N30. The phase of the input signal is inverted, and from output S1 of the inverter a logic 1 signal disables gate K186 (the remaining inputs of gate K186 at this time enter logic 1 signals), from output X of inverter N18 a logic 0 signal enters the control input of the differentiating circuit of flip-flop $\overline{Z1}$. Simultaneously from input S1 of inverter N30 a logic 1 signal enables gate K79. A Sequential clock pulses S with a negative drop in voltage opens, and with a positive enables gate K79. At the output of the gate is shaped the pulse of identical polarity and close in their parameters to the clock pulse S, which enters input E1 of the differentiating circuit of flip-flop S1. At output A of the differentiating circuit is shaped a peak positive polarity pulse, which enters input B2 and resets flip-flop S1 into the initial state.

Further description of the sequence of the drive signals through the logic circuits and the differentiating circuits will be given in a reduced description.

After inversion of the flip-flop S1 into the initial state from output S1 of inverter N30 a logic 0 signal disables gate K186.

At output of gate K186 is formed a positive voltage drop, which through the differentiating circuit sets flip-flop Z1 incrementing the Z counter. The inversion of flip-flop Z1 corresponds to the record of one (00001) into the Z counter, which works in the binary number system.

From output Z1 of inverter N79 a logic 1 signal through gate D13 is fed to the input of inverter N36. The phase of the input signal is inverted, at output $\overline{Z}$ of inverter we obtain a logic 0 signal, which through the gate D25 is fed to the input of inverter N69, (other inputs of gate D25 at this time enter logic 0 signals.) The phase of the input signal is inverted, and from output M of the inverter a logic 1 signal enters the inputs of gates K162 and K74.

Sequential clock pulses S through gate K162 and the differentiating circuit with S1=0 triggers the monostable, which after 4mS returns to the initial state.

On outputs t and $\bar{t}$ of inverters N1 and N2 of the monostable are generated short-term pulses of rectangular form and opposite polarity.

Pulse $\bar{t}$ through the differentiating circuit sets flip-flop S1. From output S1 of inverter N30 a logic 1 signal disables gate K74. Simultaneously from output S1 of the inverter a logic 1 signal enters the control input of the differentiating circuit and prevents the triggering of the monostable by Sequential clock pulses S through gate K162.

Sequential clock pulses S through gate K79 resets flip-flop S1 into the initial state. From output S1 of inverter N30 a logic 0 signal enters the input and disables gate K74. A positive voltage drop from the output of the gate through the differentiating circuit sets flip-flop LES-SCHREIB (Read - Write) into the working order. After inversion of the flip-flop at output LES of inverter N25 a logic 0 signal is generated, and at the output SCHREIB of inverter N26 - a logic 1 signal. Sequential clock pulses S through gate K162 is fed to the input of the differentiating circuit and triggers the monostable. At the outputs of inverters N1 and N2 monostable pulses t and $\bar{t}$ are generated for the correct operation of the read and write flip-flops.

A positive voltage drop of pulse $\bar{t}$ through the differentiating circuit sets flip-flop S1.

Sequential clock pulses S through gate K79 and the differentiating circuit resets flip-flop S1 into the initial state. A positive voltage drop from output S1 of inverter N30 through gate K74 and the differentiating circuit resets the read and write flip-flops into the initial state. At output SCHREIB of inverter N26 is formed a positive voltage drop, which through the differentiating circuit sets flip-flop UV. After the inversion of the flip-flop at output U of inverter N27 a logic 0 signal is generated, and at the output V of the inverter N28 - a logic 1 signal.

Sequential clock pulses S through gate K162 triggers the timing monostable t. At outputs of inverters N1 and N2 are shaped the pulses t and $\bar{t}$ with the working order of flip-flop UV and with the initial state of the read and write flip-flops.

A positive voltage drop of pulse t through the differentiating circuit sets flip-flop S1. Sequential clock pulses S through gate K79 and the differentiating circuit resets flip-flop S1 into the initial state. A positive voltage drop from output S1 of inverter N30 through gate K74 and the differentiating circuit sets the read and write flip-flops into the working order.

Sequential clock pulses S ensures the inversion of the monostable and the shaping of pulses t and $\bar{t}$ at outputs of inverters N1 and N2 with the working order of flip-flops UV and reading and writing, a positive voltage drop of pulse t through that differentiating chain sets flip-flop S1.

From output S1 of inverter N30 a logic 1 signal disables gate K84. Sequential clock pulses S through gate K79 and the differentiating circuit resets flip-flop S1 into the initial state.

From output S1 of inverter N30 a logic 0 signal enters the input and disables gate K74. A positive voltage drop from the output of the gate through the differentiating circuit resets the read and write flip-flops into their initial state. At output SCHREIB of inverter N26 is formed a positive voltage drop, which through the differentiating circuit resets flip-flop UV into the initial state. From output S1 of inverter N30 a logic 0 signal enters the input and disables gate K84. At output of inverter N33 is generated The VLS pulse of the first byte of identical polarity, equal in the duration to pulse S1.

Gate K196 is in the disabled state by the logic 0 signals of inputs $\overline{Z1}$ and S16. From the output of inverter $\overline{S16}$ a logic 1 signal enables gate K187. The VLS pulse of the first byte through gate K187 and the differentiating circuit resets flip-flop Z1 into the initial state. From output Z1 of inverter N79 a positive voltage drop through gate K188 and the differentiating circuit sets flip-flop Z2. The inversion of flip-flop Z2 into the working order corresponds to the record number 2 (00010) into the Z counter.

During the working order of flip-flop Z2 occurs the repetition of the cycle of the shaping of pulses t, $\overline{t}$, S1 and the sequential switching of the read and write flip-flops and UV. The VLS pulse of the 2nd byte through gate K187 and the differentiating circuit sets flip-flop Z1 and increases the information of the Z counter by one.

A change of the record in the Z counter from 00001 to 10000 ensures control of the bytes of memory unit in the forward sequence. After control of the 15th byte the position of flip-flops corresponds to the record number 15 (01111) in the Z counter. The VLS pulse of the 15th byte through gate K187 and the differentiating circuit resets flip-flop Z1 into the initial state. Fromoutput Z1 of inverter N79 a positive voltage drop through gate K188 and the differentiating circuit resets flip-flop Z2 into the initial state. From output Z2 of inverter N81 a positive voltage drop through gate K190 and the differentiating circuit resets flip-flop Z4 into the initial state. From output Z4 of inverter N83 a positive voltage drop through gate K193 and the differentiating circuit resets flip-flop Z8 into the initial state. From output Z8 of inverter N84 a positive voltage drop through the differentiating circuit sets flip-flop Z16 into the working order.

The information of the Z counter increases by one and corresponds to the record number 16 (10000) in the binary number system. The position of the Z counter ensures control of the 16th byte of the memory unit. After the inversion of the Z16 flip-flop

from output Z16 of the flip-flop a logic 1 signal disables gate K196. From output S16 of inverter N87 a logic 1 signal disables gate K212. From output $\overline{S16}$ of inverter N88 a logic 0 signal disables the operation of gate K187. Simultaneously a logic 0 signal from output S16 of the inverter enters the control input and prepares for the operation the differentiating circuit of the Z16 flip-flop. The VLS pulse of the 16th byte through the differentiating chain resets flip-flop Z16 into the initial state and turns off the Z counter.

III.1.2. Reverse counting of the Z counter.

During a straight cycle of the Z counter flip-flop F1 is reset. The inversion of flip-flop F1 through one of gates K140, K144, K147, K183 and K186 ensures the specific mode of operation of the functional diagram in the short-term conducting state of gates K75 or K76.

With the output of the disabled gates K75 or K76 a logic 1 signal is fed to the input of gate D10 of the memorizing circuit.

After inversion of the flip-flop F1 into the working order, from output F1 of inverter N63 a logic 1 signal is fed to the input of gate K77 and enables the memory circuit.

The memorizing circuit formed from gates D10 and K77, inverters N23 and N24 retain the short-term logic 1 signals from the output of gates K75 or K76 to the inputs of gate D10.

In the initial state of the memorizing circuit at output $\overline{R\ddot{u}}$ of inverter N23 a logic 1 signal is generated, and at the output Rü of inverter N24 a logic 0 signal.

A logic 1 signal from the output of gates K75 or K76 is fed to the input of gate D10 and in the short-term switches the memorizing circuit into the working order.

At output $\overline{R\ddot{u}}$ of inverter N23 a logic 0 signal is generated, and at the output Rü of inverter N24 a logic 1 signal, which disables gate K77. From the output of the disabled gate K77 a logic 1 signal is fed to the input of gate D10 and ensures the working order of the memory circuit, until flip-flop F1 is located in running order, I.e. Thus far input F1 of gate K77 enters a logic 1 signal.

From output $\overline{R\ddot{u}}$ of inverter N23 a logic 0 signal is fed to the input of inverter N24 and also disables the operation of gates K188, K190, K193 and K212. From output Rü of inverter N24 a logic 1 signal enables gate K195.

Pulse S1 through gate K195 and the differentiating circuit sets flip-flop incrementing the Z counter.

The working order of the Z16 flip-flop corresponds to record number 16 (10000) in the Z counter and to control of the 16th byte of the memory unit.

From the output of the Z16 flip-flop a logic 1 signal disables gate K196. From output S16 of inverter N87 a logic 1 signal enters input gate K212.

During the initial state of flip-flops Z1, Z2, Z4, Z8 gate K212 is disabled when a logic 0 signal inputs $\overline{R\ddot{u}}$. At output $\overline{S16}$ of inverter N88 a logic 1 signal is generated. Usually with the reverse counting of the Z counter the flip-flop VER (shift) is located in running order.

From output $\overline{VER}$ of inverter N67 a logic 0 signal enters the collector input, setting and blocking flip-flop UV (V ?) .

Simultaneously from output VER of inverter N68 a logic 1 signal enters the control input of the differentiating circuit and disables the operation of gate K150 preventing the reset of flip-flop F1.

During the working order of flip-flop Z16 occurs in the usual sequence the shaping of pulses t, $\bar{t}$, S1 and switching of flip-flop LES-SCHREIB.

The working order of flip-flop UV ensures the shaping of VLS pulses through gate K84 and the inverters N32 and N33 from each second S1 pulse.

The VLS pulse of the 16th byte through gate K187 and the differentiating circuit sets flip-flop Z1 into the working order.

A positive voltage drop from output $\overline{Z1}$ of inverter N78 through gate K189 and the differentiating circuit sets flip-flop Z2 into the working order. A positive voltage drop from output $\overline{Z2}$ of inverter N80 through gate K191 and the differentiating circuit sets flip-flop Z4 into the working order. A positive voltage drop from output $\overline{Z4}$ of inverter N82 through gate K192 and the differentiating chain sets flip-flop Z8 into the working order.

In running order one of the flip-flops Z1, Z2, Z4, Z8 at outputs $\overline{Z1}$, $\overline{Z2}$, $\overline{Z4}$, $\overline{Z8}$ of the corresponding inverters generates a logic 0 signal, which enters one of the inputs and disables gate K196. As a result the disabled state of gate K196 at output S16 of inverter N87 a logic 0 signal is generated.

The working order of flip-flops Z1, Z2, Z4, Z8, Z16 corresponds to record number 31 (11111) in the Z counter and to control of the 15th byte of memory unit. Switching flip-flop LES-SCHREIB, in the shaping of pulses t, $\bar{t}$, S1, VLS for the 15th byte occurs in the usual sequence.

The VLS pulse of the 15th byte through gate K187 and the differentiating circuit resets flip-flop Z1 into the initial state and decreases the information of the Z counter by one. Gate K188 is disabled with a logic 0 signal at input $\overline{R\ddot{u}}$. Consequently, a positive voltage drop from output Z1 of inverter N79 does not change the state of gate K188 and flip-flop Z2. The working order of flip-flops Z2, Z4, Z8, Z16 corresponds to record number 30 (11110) in the Z counter and to control of the 14th byte of memory unit. The VLS pulse of the 14th byte through gate K187 and the differentiating circuit sets flip-flop Z1 into the working order. A positive voltage drop from output $\overline{Z1}$ of inverter N78 through gate K189 and the differentiating circuit resets flip-flop Z2 into the initial state and decreases the information of the counter by one.

The working order of flip-flops Z1, Z4, Z8, Z16 corresponds to record number 29 (11101) in the Z counter and to control of the 13th byte of memory unit.

A sequential change in the positions of the Z counter from 11111 to 10001 ensures control of the bytes of memory unit in a reverse sequence.

In one of the bytes during the reverse counting of the Z counter at output X of inverter N18 a logic 1 signal is generated, which enables gate K158. Pulse VLS through gate K158 and the differentiating circuit when S16=0 resets flip-flop VER into the initial state. From output VER of inverter N68 a logic 0 signal enters the control input and prepares for the operation the differentiating circuit of gate K150. After control of the 1st byte the position of the flip-flops correspond to the record number 17 (10001) in the Z counter. Pulse VLS of the 1st byte through gate K187 and the differentiating circuit resets flip-flop Z1 into the initial state, the position of the flip-flops correspond to record number 16 (10000) in the Z counter and to control of the 16th byte of the memory unit. After the inversion of flip-flop Z1 into the initial state from output Z1 of inverter N78 a logic 1 signal disables gate K196. From output S16 of inverter N87 a logic 1 signal enables gate K150. The VLS pulse of the 16th byte through gate K187 and the differentiating circuit ensures the sequential inversion of flip-flops Z1, Z2, Z4, Z8 into the working order.

The working order of flip-flops Z1, Z2, Z4, Z8, Z16 corresponds to record number 31 (11111) in the Z counter and to control 15th byte of memory unit.

The flip-flops of the Z counter in the process of sequential inversion from outputs $\overline{Z1}$, $\overline{Z2}$, $\overline{Z4}$, $\overline{Z8}$ send logic 0 signals to the inputs and shut gate K196. At output S16 of inverter N87 is formed a positive voltage drop, which through gate K150 and the differentiating circuit with VER=0 resets flip-flop F1 into the initial state, from output F1 of inverter N63 a logic 0 signal enters the input and disables gate K77 of the memory outline. From the output of gate K77 a logic 0 signal is fed to the input of gate D10 and switches the memorising circuit into the initial state. After switching the output $\overline{R\ddot{u}}$ of inverter N23 begins to be generated a logic 1 signal, at output Rü of inverter N24 a logic 0 signal.

From output $\overline{R\ddot{u}}$ of inverter N23 a logic 1 signal enables gates K188, K190, K193 and K212.

From output Rü of inverter N24 a logic 0 signal disables gates K189, K191 and K192.

Pulse VLS of the 15th byte through gate K187 and the differentiating circuit ensures the sequential inversion of flip-flops Z1, Z2, Z4, Z8 into the initial state. Flip-flop Z16 remains in running order, pulse VLS of the 16th byte through the differentiating circuit with $\overline{S16}$=0 resets flip-flop Z16 into the initial state and turns off the Z counter.

III.1.3.   Operational control of the registers and bytes of the memory unit.

Each register of the memory unit is divided into two lines of 8 ferrite cores (Fig. 28, 29).

In the upper line of a register ferrite cores 8, 9, 10, 11, 12, 13, 14 and 15 are placed, in the lower line - ferrite cores 16, 1, 2, 3, 4, 5, 6 and 7.

Control of the ferrite cores of a register is performed by gates K12 ÷ K23, the operation of which is governed by the Z counter.

Register control is performed by gates K6 - K11, operation of which is governed by the schematic of the arithmetic-logic unit. Prior to beginning the introduction and completion of operations the functional diagram of the arithmetic-logic unit ensures control of the MR register.

With the operation of the electrical control circuit of ferrite cores let us examine the principle of reading and writing to the four ferrite core planes the 4, 8 and the 12th of the bytes of the MR register (Fig. 28, 29).

From output MRS of inverters N29 and N38 a logic 1 signal enables gate K6. During operation of the Z counter flip-flop Z4 sets into the working order. From outputs $\overline{Z1}$, $\overline{Z2}$ of inverters N78 and N80 logic 1 signals are generated. They enter the inputs and prepare for the operation of gate K23. From output Z4 of inverter N83 a logic 1 signal enables gates K18 and K19. From output $\overline{Z8}$ the inverter N85 generates a logic 1 signal which enables gates K12 and K13. Flip-flop LES-SCHREIB is reset. From output LES of inverter N25 a logic 1 signal enables gates K12 and K18. Pulse t of the 4th byte through gates K23, K18, K6 and K12 produces the starting of the corresponding four ferrite cores driver stages. Current pulse $\frac{Im}{2}$ of the driver stages (Fig. 28) with the 4th and 12th bytes flows in the circuit: Ov_{sp} exciting stage Y910, wire S4L, the sensing wire of bytes, a diode, driver stage Y911, 40ohm resistor, $-U_{sp}$.

The current pulse $\frac{Im}{2}$ in the driver stages (Fig. 29) of register MR and lower line flows in the circuit: Ov_{sp}, driver stage Y910, wire Z8L, sensing wire of the register line, a diode, driver stage Y911, 40ohm resistor, $-U_{sp.}$ The identical direction of the half-currents of the readout $\frac{Im}{2}$, which take place through the ferrite cores only of 4th byte create the summed current Im, ensures the reversal of polarity of the corresponding ferrite cores and the readout of the written information. The readout of the information of the 12th byte occurs analogously with readout in the 4th byte. In this case instead of gate K12 enabling the corresponding driver stage Y910 it occurs through gate K14. The readout of the information of the 8th byte occurs analogously with the readout of 12th byte. In this case instead of gate K18 enabling the corresponding driver stage Y910 it occurs through gate K16.

The process of reading out stored magnetic information only occurs in the groups of four ferrite cores in which a logical 1 is written. The groups of four cores with a stored 0 do not reverse their magnetism.

As a result of the polarity reversal in the cores an EMF is induced on the read wires, which enters the inputs of the corresponding read amplifiers (Fig. 7)
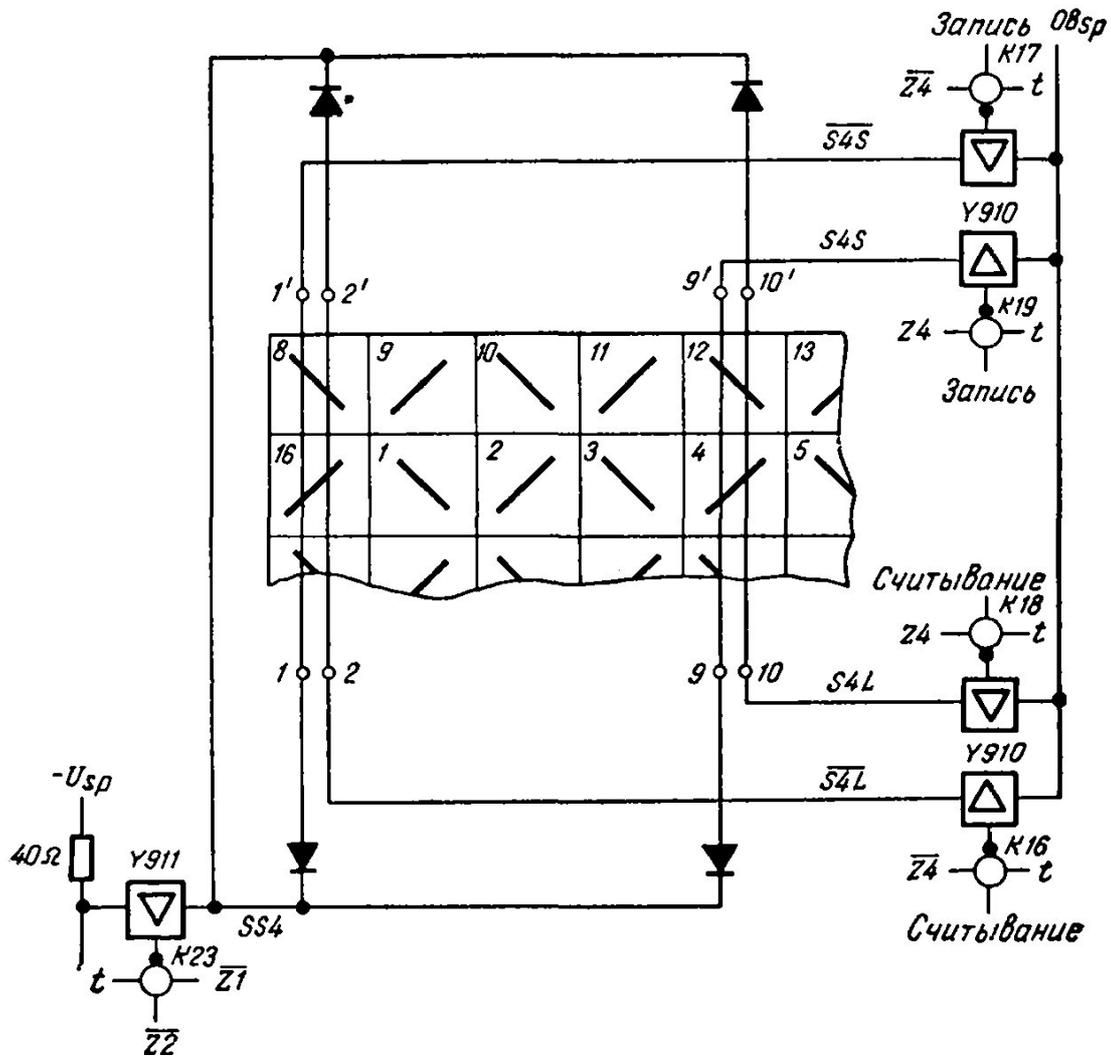
Fig, 28. Schematic diagram of the passage of half-currents for the
reading and writing of bits.

The outputs HV1 - HV8 of the read amplifiers are positive polarity pulses. From the output of the read amplifiers the pulses enter the differentiating circuits and ensure the inversion of the corresponding four flip-flops of register A into the working order.

The record of information into the 4th byte occurs analogously with readout by the currents $\frac{\text{Im}}{2}$ of opposite direction.

Flip-flop LES-SCHREIB is located in running order. From output SCHREIB of inverter N26 a logic 1 signal enables gates K13 and K19.

Pulse t of the 4th byte through gates K6, K23, K19 and K13 enables the drivers of the corresponding four stages of ferrite cores. Current pulse $\frac{Im}{2}$ of the driver stages (Fig. 28)

The 4th and twelfth bytes flow in the circuit: 0Vsp, driver stage Y910, wire S4S, the write wire of the bytes, diode, driver stage Y911, 40ohm resistor, -U$_{sp}$.
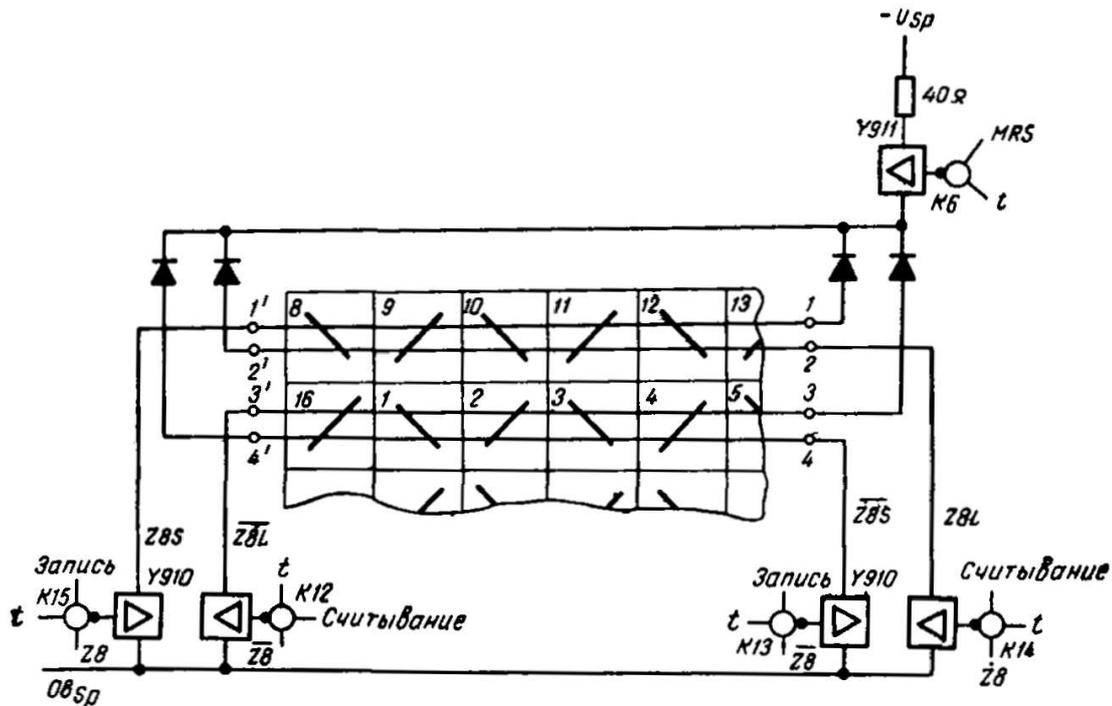
Fig. 29. Schematic diagram of the passage of half-currents for the
reading and writing of a register.

The current pulse $\frac{Im}{2}$ in the driver stages (Fig. 29) of register MR and lower line flows in the circuit: OV$_{sp}$, driver stage Y910, the wire $\overline{Z8S}$, the wire of the record of the line of register, the diode, driver stage Y910, 40ohm resistor, -U$_{sp}$.

The identical direction of the write half-currents $\frac{Im}{2}$, which take place through the ferrite cores of only the 4th byte, create the summed current Im, which ensures the polarity reversal of the ferrite cores and writing of the corresponding information in the absence of the opposite current from the inhibit drivers. The opposite inhibit current of the bytes of the [four bits] $\frac{Im}{2}$ flows through the ferrite cores and creates the resulting current $\frac{Im}{2}$. The resulting current for the polarity reversal of the ferrite cores is not produced.

The writing of information into the 12th byte occurs analogously with writing into the 4th byte. In this case instead of gate K13 enabling the corresponding driver stage Y910, it occurs through gate K15.

The writing of information into the 8th byte occurs analogously with writing into the 12th byte, but in this case instead of gate K19 enabling the corresponding driver stage Y910 it occurs through gate K17. In the process of writing information only the ferrite cores of the four bits reverse magnetism when a zero is written. The four bits of cores written with a one do not reverse magnetism.

Control of write inhibits operations occurs through gates K24, K1, K2 and K25 (Fig. 30, see supplementary sheet).

Write inhibit current pulses are shaped at outputs BL1, BL2, BL4, BL8 of the inhibit drivers and respectively enter the first, second, third and fourth memory arrays. Write inhibit pulses prevent the reversal of polarity of the corresponding four ferrite cores.

III.2.   Entry of digital information.

The input of digital information into the arithmetic-logic unit occurs by consecutive usage of the corresponding keyboard, beginning from the high-order digit of the number. In this example the assigned degree of accuracy is set by rotating the decimal point position switch to the number 3. Prior to entering any information the machine is reset into operating conditions and it is completely prepared for executing arithmetic operations. Let us examine the sequence of the operation of the overall functional (logical) diagram of machine based on the example of entering the numbers 763, 542.

In the initial state of the keyboard input unit (Fig. 19) a logic 0 signal from the power supply through connector 5V3, series-connected contacts of the digital and functional keyboard and connector 7V3 arrives at the K inputs of the Keyboard diagram (Fig. 21, 30 (see supplementary sheet)). From output $\overline{KO}$ of the keyboard diagrams a logic 0 signal through a 4,7k resistor is fed to the input of inverter N61 (Fig. 30 see supplementary sheet). From output ST + K0 of the inverter N61 a logic 1 signal enables the operation of gate K186 and the Z counter.

The entry of the high-order digit of the number is ensured by pressing the key for number 7, which changes the position of the corresponding contact and disconnects the logic 0 signal chain from the $\overline{K}$ input of the keyboard diagram. At output $\overline{KO}$ of the keyboard diagram a logic 1 signal is generated, which through the 4,7k resistor is fed to the input of inverter N61 (Fig. 30 see supplementary sheet). The phase of the input signal is inverted, and from output ST + K0 of the inverter a logic 0 signal enters the input and disables gate K186. This disables the Z counter.

The closing contacts of the digital "7" key ensures the connection of a logic 0 signal from the power source through the connector 5V3 (Fig. 19), the consecutively connected contacts of the functional keyboard section and the connector 7V4 to the input 7K of the encoder diagram (Fig. 20).

From the input of the keyboard encoder diagram a logic 0 signal through the diodes of the keyboard encoder and the filter circuits L10, L13, L11, L14.

From the output Z/0 of the keyboard diagram a logic 0 signal enters through a diode to the input of monostable ST (flip-flop Schmitt) and then to the controlling input of the differentiating circuit for flip-flop VER (inversion of the monostable ST from a logic 0 input signal proceeds with a delay of 10ms.)

Simultaneously from outputs Z/10, Z/20, Z/40 of the keyboard filter circuits L13, L11, L14 logic 0 signals enter the controlling inputs enabling the differentiating circuits of the flip-flops for bits E1, E2 and E4 of register E.

After the disconnection of the Z counter, logic 0 signals from outputs Z1, Z2, Z4, Z8 and Z16 of inverters N79, N81, N83, N84 and flip-flop Z16 are fed to the inputs of gate D13. From the output of the gate a logic 0 signal enters inverter N36, the phase of the input signal is inverted, from output $\overline{Z}$ of the inverter a logic 1 signal enters the input and prepares for the operation gate K137. Pulses S1 through gate K137 enter the input of inverter N55. At the output of inverter N56 the signal EING (entry) is formed a pulse train of identical polarity, similar in form to the S1 pulses. (With the series connection of two inverters the phase of the input signal from the input of the 1st inverter to the output of the 2nd inverter does not change.)

The series of pulses EING are fed to the inputs of the corresponding differentiating circuits and invert flip-flops VER, E1, E2 and E4. The inversion of flip-flops E1, E2 and E4 corresponds to writing the number 7 (0111) into the four flip-flops of register E. From the VER output of inverter N68 a logic 1 signal disables gate K86 (second gate input $\overline{F3}$=1).

From the output of gate K86 a logic 1 signal through gate D14 is fed to the input of inverter N34. From output HV of the inverter a logic 0 signal disables the operation of the V507 read amplifiers.

As a result of the inversion of flip-flop VER a logic 0 signal from output $\overline{VER}$ of inverter N67 enters the collector input, setting and blocking in running order the flip-flop UV. From the output of flip-flop VF a logic 1 signal enables gate K84 for the signal VLS. Monostable ST is inverted into the working order after the pulse delay time. From the output of the monostable a logic 0 signal $\overline{ST}$ disables gate K137, which terminates the series of EING pulses.

Simultaneously the logic 0 signal $\overline{ST}$ is fed to the input of inverter N61. The phase of the signal is inverted, and from output ST + K0 the logic 1 signal enables gate K186. The inversion of monostable ST into the reset state occurs as a result the release of a digital key and breaking of the corresponding contact, pulse S1 through gate K186 and differentiating circuit sets flip-flop Z1 incrementing the Z counter. From output Z1 of inverter N79 a logic 1 signal through gate D13 is fed to the input of inverter N36. From the Z output of the inverter a logic 0 signal through gate D25 is fed to the input of inverter N69. (The remaining inputs of the gate D25 at this time enter logic 0 signals). From the output of the inverter a logic 1 signal inputs K162 and ensures the shaping of pulses MS.

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Before the switching of functional keys at outputs of the gates D11 and D15 are generated logic 0 signals, which are fed to the inputs of inverters N29 and N38. At outputs of the inverters is generated a logic 1 signal MRS, which governs the operation of the MR register. The position of the Z counter (00001) corresponds to control of the four bits of the 1st byte of the MR register. Flip-flop LES-SCHREIB is reset. From output LES of inverter N25 a logic 1 signal enables gates K12 and K16 to enable the driver stages for the readout of information.

Clock pulse S through gate K162 by a positive voltage drop triggers the timing monostable t. At the output of inverter N2 a 4uS pulse t with a duration of 4uS is generated, which through gates K6, K12, K16 and K20 enables the corresponding driver stages and thereby the readout of the stored information 0000 from the four ferrite core planes of the 1st byte of the MR register.

Simultaneously pulse $\bar{t}$ from the output of inverter N1 through differentiating circuit sets flip-flop S1 into the working order.

From output S1 of inverter N30 a logic 1 signal enables gate K79 and enable/disables gate (?) K74. Sequential clock pulses S through gate K79 and the differentiating circuit resets flip-flop S1 into the initial state. A positive voltage drop of pulse S1 through gate K74 and the differentiating circuit sets flip-flop LES-SCHREIB into the working order. From output SCHREIB of inverter N26 a logic 1 signal enables gates K13 and K19 of the write drivers. Simultaneously from output SCHREIB a logic 1 signal enables gates K24, K1, K2 and K25 of the inhibit driver stages.

The flip-flops E1, E2 and E4 of register E are located in running order. From the outputs of flip-flops E1, E2 and E4 the signals of the 1st through the gates D1, D2 and D3 are fed to the inputs of inverters N4, N6 and N8. The phase of the entered signals is inverted, from outputs C1, C2 and C4 a logic 0 signal disables the operation of gates K24, K1 and K2 of the inhibit driver stages of the 1st, 2nd and 3rd bits of the four ferrite core planes.

The flip-flop E8 is reset. From output E8 of inverter N21 a logic 0 signal through gate D4 is fed to the input of inverter N10. The phase of the entered signal is inverted, from output C8 a logic 1 signal enables gate K25 of the inhibit driver stage of the 4th byte of the four ferrite core planes. Sequential clock pulses S through gate K162 set monostable t. At the output of inverter N2 is generated the pulse t, which through gates K6, K17, K13 and K20 enables the write driver stages. Simultaneously pulse t through gate K25 will enable the inhibit driver stage, at the output of which it forms an inhibit pulse for the 4th bit of the four ferrite core planes.

From the output S1 of the N30 inverter, The l signal enters the inputs, opens the circuit To 79 and prepares the circuit To 74. Another clock pulse S through the circuit K79-and differentiating circuit overturns trigger S1 to its original state. Positive pulse voltage drop S1 via K74 circuit and differential circuit tilt trigger LES-SCHREIB in working condition. From THE schreib output of the N26 inverter, The l signal enters the input and prepares for the operation of the K13, K19 circuit to start the exciting information recording stages. Simultaneously with the output of SCHREIB, the signal L enters the inputs and prepares for the operation of the K24, K1, K2, K25 circuits of the recording ban stages.

The current pulses of the write stages produce a reversal of polarity in cores 1, 2, 3 of the four ferrite core planes, which corresponds to writing the number 7 (0111) into the 1st byte of the MR register.

Simultaneously from the output of inverter N1 pulse $\bar{t}$ through a differentiating circuit sets flip-flop S1 into the working order. From output S1 of inverter N30 a logic 1 signal disables gates K74 and K84 and enables gate (?) K79. Sequential clock pulses S through gate K79 and the differentiating circuit resets flip-flop S1 into the initial state, from output S1 of inverter N30 a logic 0 signal enters the inputs and shuts gates K74 and K84, A positive voltage drop from the output of gate K74 through the differentiating circuit resets flip-flop LES-SCHREIB into the initial state. Simultaneously with the shaping of the pulse S1 through gate K84 at output of inverter N33 is shaped the pulse VLS, which through gate K187 and the differentiating circuit resets flip-flop Z1 into the initial state.

At output Z1 of inverter N79 is formed a positive voltage drop, which through gate K188 and the differentiating circuit sets flip-flop Z2 into the working order.

The position of the Z counter (00010) corresponds to control of the four bits of the 2nd byte of the MR register. The mode of operation of the functional diagram in the process of reading and writing the 2nd and subsequent bytes does not change.

The VLS pulse of the 15th byte through gate K187 ensures the sequential inversion of flip-flops Z1, Z2, Z4 and Z8 into the initial state, and Z16 - into the working order. From flip-flop Z16's output a logic 1 signal disables gate K196, from the output of the gate a logic 1 signal is fed to the input of inverter N86. From output Z16 of inverter N87 a logic 1 signal prepares for the operation of gate K160 and disables gate K212.

From the output of gate K212 a logic 1 signal is fed to the input of inverter N88.
From output $\overline{S16}$ of inverter N88 a logic 0 signal enters the input and disables gate K187.

Simultaneously from output $\overline{S16}$ a logic 0 signal enters a control input and enables the differentiating circuit of the Z16 flip-flop.

The VLS pulse of the 16th byte through the prepared differentiating circuit resets flip-flop Z16 into the initial state and turns off the Z counter. A positive voltage drop of the Z16 flip-flop output through another differentiating circuit (with $\overline{VER}$=0) sets flip-flop F3 into the working order. From output $\overline{F3}$ of inverter N64 a logic 0 signal enters the input and disables gate K86. Simultaneously a VLS pulse through gate K160 [K161?]* and the differentiating circuit (with ÜBER=0) resets flip-flop VER into the initial state. A positive voltage drop of the VER output of inverter N68 through the differentiating circuit of flip-flop UV it resets it into the initial state.

* - Gate K160 is split over boards 8, 9 and 10, but on board 9 it seems to be numbered K161. The three connections required are all on pin 57 (B26) of each board on the backplane but are named on the German logic diagrams thus :-

Board 8 = K($\overline{VOR}$, VLS, $\overline{\overline{A8}}$, $\overline{R}$, $\overline{RU}$, S16)

Board 9 = K($\overline{VOR}$, VLS, $\overline{\overline{A8}}$, R, $\overline{RU}$, S16, AUSG)   (Inverted R, added AUSG)

Board 10 = K($\overline{VOR}$, VLS, $\overline{A8}$, $\overline{R}$, $\overline{RU}$, $\overline{AUSG}$)   (S16 missing, inverted AUSG)

On the www.soemtron.org diagrams this net has been called \A8-RU. $\overline{A8\text{-}RU}$

After disconnection of the Z counter the pulse S1 through gate K186 and the differentiating circuit (X=0) sets flip-flop Z1 incrementing the Z counter.

The following number when entered is written into register MR which is then displayed by the operation of the Z counter.

Entering the second and following numbers of an example proceeds in a sequence, analogous to entering the first number of an example but with some changes, which consist of the following:

1)   The working order of flip-flop F3 during the readout of information in notebook each byte ensures the disabled state of gate K86 and, as a result, a logic 1 signal at output HV of inverter N34, which enables and prepares the read amplifiers V507 for operation.

2)   After the switching on the counter and pulse t with the initial state of flip-flop LES-SCHREIB ensures the reversal of polarity of cores and the readout number 7 (0111) from the 1st byte of the MR register. On reading the four ferrite core planes an EMF is directed, which inputs and excites amplifiers of the 1, 2 and 3rd of bits. At the output of the read amplifiers are short-term pulses, shaped through differentiating circuits, which by a positive voltage drop set flip-flops A1, A2 and A4 into the working order.

3)   Pulse t following the usual sequence ensures the recording of the number 6 (0110) from the four flip-flops of register E into the four bits of the 1st byte of the MR register.

4)   Pulse VLS of the 1st byte through the appropriate differentiating circuits set flip-flops A1, A2 and A4 into initial order. Positive drops in the voltage of outputs A1F, A2F and A4F are fed to the inputs of the differentiating circuits of flip-flops E1, E2 and E4 with the enable inputs SUB.

At the outputs of the differentiating circuits with SUB=0 positive polarity pulses, respectively set flip-flop E1 and does not change the state of flip-flops E2 and E4. From outputs A1, A2, A4 of inverters N5, N7 and N9 logic 1 signals enter the controlling inputs and block the operation of the differentiating circuits for the inversion of flip-flops E1, E2 and E4 into the initial state. Simultaneously with the inversion of the four flip-flops of register A into the initial state pulse VLS of the 1st byte enters the inputs of the differentiating circuits and does not invert flip-flops E2 and E4 into the initial state.

Consequently, the inversion of the four flip-flops of registers A and E from the pulse VLS ensures the re-writing of the information of the four flip-flops of register A into the four flip-flops of register E. The resetting of the four flip-flops of register E into the initial state from the pulse VLS proceeds only when to the controlling inputs A1 ÷ A8 of the corresponding differentiating circuits enters a logic 0 signal, I.E. when flip-flop A is in the initial state, and the corresponding flip-flop E is in running order.

5) After switching the Z counter for the reading and writing in the 2nd byte the first pulse t ensures readout 0000. The second pulse t ensures the record of the number 7 (0111) into the four bits of the 2nd byte of the MR register. The flip-flops of the A register are in the initial state, therefore, pulse VLS resets the four flip-flops of register E into the initial state.

6) Further operation of the Z counter flows in the usual sequence.

7) Entry of the next number occurs in a sequence, analogous to the input of the second number of an example, I.E. with a one byte shift to the left of the previously entered number 76. As a result of the entry of three numbers, into the four bits of the MR register will be written the number 763 (0111 0110 0011). Flip-flop F3 remains set to the start of the corresponding functional key.

III.2.1. Decimal point key "comma".

The position of the decimal point switch through contacts G21, G22, G24, G28 of the switch wafers where logic 0 signals are generated, which through the appropriate encoder circuit diagram are fed to the inputs of the differentiating circuits and govern the start of the Z counter (Fig. 22). The start of the Z counter and the selection X = (16-K) of the byte of memory unit (where K corresponds to the accuracy of the degree of calculation) occurs with the operation of the "decimal point" key. In accordance with the example K = 3, at outputs G21, G24, G28 we obtain a logic 0 signal, which through connectors 4V5, 6V5, 7V5 and the installation of arithmetic-logic unit enter filters L7, L9, L4 (Fig. 30 see supplementary sheets). From the filter outputs G210, G240, G280 logic 0 signal enters the control inputs and prepare for the operation the differentiating circuits of the corresponding Z counter flip-flops.

The "decimal point" key is included after the integer part of a number. Usually the operation of the "decimal point" key occurs when the quantity of digits in the fractional part of the number is greater than the established degree of accuracy of calculations. If a quantity of decimal digits of the fractional part of the number corresponds to the established degree of accuracy of calculations, operation the "decimal point" key is not required.

After pressing the "decimal point" key a sequence, analogous to the description of the operation of a digital key, occurs the switching of the corresponding contact of the input unit and the preparation of the arithmetic-logic unit schematic for the disconnection of the Z counter.

The switched contact of the "decimal point" key through connector 1V4 and the encoder diodes connects a logic 0 signal to the inputs of the numeric encoder and filters L10, L14 and L12, from the outputs Z/0, Z/40 and Z/80 of the diagrams a logic 0 signal enter the inputs and enable the operation of the differentiating circuits of flip-flops VER, E4 and E8.

From output ST + K0 of inverter N61 a logic 0 signal disables the operation of gate K186. As a result after the end of calculations the start of the Z counter through gate K186 does not occur.

At output $\overline{Z}$ of inverter N36 a logic 1 signal is generated which enables gate K137. S1 pulses enter the input of gate K137, as a result of which at output of inverter N56 is formed the pulse train EING (entry). The serial EING pulses through the differentiating circuits set flip-flops VER, E4 and E8 into the working order.

The working order of flip-flops E4 and E8 ensures the recording into the four bits of register E the number 12 (1100), which it is conditionally customary to assume as the X12 marker. From output $\overline{VER}$ of inverter N67 a logic 0 signal enters the collector input, it sets and retains in running order flip-flop UV.

Simultaneously from output $\overline{VER}$ a logic 0 signal enters the control input of the differentiating circuit and prepares the inversion of flip-flop ÜBER (overflow) into the working order.

From the flip-flop outputs E4 and inverters N21 E8 and N68 VER, logic 1 signals disable gate K59. From the output of gate K59 a logic 1 signal through gate D5 is fed to the input of inverter N17. At output "X" of inverter N18 a logic 1 signal is generated, which enters the control input of the differentiating circuit of flip-flop Z1 and disables the operation of gate K186. Simultaneously from output "$\overline{X}$" of inverter N17 a logic 0 signal enters the control input and prepares for the operation the differentiating circuit of flip-flop F1. With the operation of the "decimal point" key a logic 0 signal from output Z/0 of the keyboard filter L10 enters the keyboard monostable and sets flip-flop ST in working order for 10mS. From output ST + K0 of inverter N61 a logic 1 signal enables gate K186.

Pulse S1 through gate K186 and the differentiating circuit sets flip-flop F1 into the working order. From output F1 of inverter N62 a logic 1 signal disables gate K138. From the output of gate K138 a logic 1 signal passes through gate D26 to inverter N54. At output G2 of inverter N54 is formed a positive voltage drop, which via the differentiating circuits, sets flip-flops Z1, Z4, Z8 and Z16. The position of the Z counter corresponds to record number (11101) and to control of the 13th byte of the MR register. Simultaneously a positive voltage drop of output G2 through the differentiating circuit with $\overline{VER}$=0 sets flip-flop ÜBER into the working order. At output ÜBER of inverter N22 a logic 1 signal is generated, which enters the control input of the differentiating circuit of flip-flop VER and disables the operation of gate K160.

In the usual sequence the read and write cycles from the four bits of register E rewrite the X12 marker into the 13th byte of the MR register and ensure error and disconnection of the Z counter with pulse VLS of the 16th byte. Flip-flop VER remains in running order, I.E. The operation of gate K160 from the pulse VLS is blocked by a logic 1 signal at the controlling input ÜBER of the differentiating circuit.

After the disconnection of the Z counter, from output $\overline{Z}$ of inverter N36 a logic 1 signal enables gate K66. Clock pulse S through gate K66 and the differentiating circuit with MUL = 0 resets flip-flop ÜBER into the initial state.

The controlling input R of the differentiating circuits of the four bits of the register E flip-flops enter a logic 0 signal.

A positive voltage drop from the ÜBER output of inverter N22 enters the inputs of the differentiating circuits and set flip-flops E2 an E8 into the working order. The working order of flip-flops E2 and E8 corresponds to writing into the four bits of register E the number 10 (1010), which it is conditionally customary to assume as the X10 marker .

Sequential pulses S1 through gate K186 and the differentiating circuit with X=0 set flip-flop Z1 incrementing the Z counter.

In the usual sequence the read and write cycles rewrite the X10 marker from the four bits of register E into the 1st byte of the MR register and ensure a left-shift to one byte of the previously entered X12 marker and the digits of the integer part of the number, as a result the operation of the "decimal point" key the marker will be written into the four planes of the MR register with the integer part of the number of - $00X_{12}000000000763X_{10.}$

0000 0000 1100 0000 0000 0000 0000 0000 0000 0000 0000 0000 0111 0110 0011 1010

Pulse VLS of the 16th byte through the differentiating circuit with $\overline{S16}$ =0 resets flip-flop Z16 into the initial state and turns off the Z counter. Simultaneously pulse VLS through gate K160 and the differentiating circuit with ÜBER = 0 resets flip-flop VER into the initial state.

A positive voltage drop of the VER output of inverter N68 through the differentiating circuit resets the UV flip-flop into the initial state.

Flip-flops F1 and F3 remain set. Sequential pulses S1 through gate K186 and the differentiating circuit sets flip-flop Z1 incrementing the Z counter.

The cycles of the Z counter occur before the switching of a digital or functional key and ensure the display of digital information, X10 marker and sign of the number.

III.2.2. Input of a fractional part of a number.

Entry of each digit of the fractional part of a number occurs in a sequence, analogous to the description of the entry of the digits of the integer part of a number, with the shift to one byte to the left of the previously entered numbers and X12 and X10 markers.

As an example after the entry of the number 4 (0100) the X12 marker (1100) will be written into the four bits of the 16th byte of the MR register - $X_{12}000000000763X_{10}54$.

1100 0000 0000 0000 0000 0000 0000 0000 0000 0000 0111 0110 0011 1010 0101 0100

As a result of the entry of the number 2 (0010), I.E. The last fractional digit part of the example number, the X12 marker is rewritten from the four bits of 16th byte of the MR register into the four flip-flops of register A.

Flip-flops A4 and A8 invert into the working order. From the $\overline{A8}$ flip-flop output a logic 0 signal disables the operation of gate K160. As a result flip-flop VER is not inverted from the VLS pulse of the 16th byte.

From the outputs of inverters N9 and N11 logic 1 signals enter inputs A4, A8 and disable gate K56. From the output of gate K56 a logic 1 signal through gate D5 is fed to the input of inverter N17.

From output $\overline{X}$ of inverter N17 a logic 0 signal is fed to the input of inverter N18. From output X of inverter N18 a logic 1 signal enters the control input of the differentiating circuit and blocks the inversion of flip-flop Z1 through gate K186. Pulse VLS of the 16th byte through the differentiating circuit reset flip-flops A4 and A8 into the initial state and store the X12 marker into the four flip-flops of register E. From the outputs of flip-flops A4 and A8, logic 0 signals disable gate K56. From outputs E8 of inverter N21 a logic 1 signal disables gate K59. As a result at output X of inverter N17 there remains a logic 0 signal, at output X of inverter N18 - a logic 1 signal. Simultaneously the VLS pulse of the 16th byte through a differentiating circuit resets flip-flop Z16 into the initial state and turns off the Z counter. After the entry of the last figure of the fractional part of the number, into the four planes of the MR register will be stored the number $000000000763X_{10}542$ with the X10 marker.

(0000 0000 0000 0000 0000 0000 0000 0000 0000 0111 0110 0011 1010 0101 0100 0010)

After disconnection of the Z counter sequential pulse Y disable gate K76.

From the output of gate K76 a logic 1 signal is fed to the input of gate D10 and switches the memorising circuit into the working order. As a result of the switching at the $\overline{Ru}$ output of inverter N23 we obtain a logic 0 signal, at the Rü output of inverter N24 - a logic 1 signal. From the Rü output of the inverter a logic 1 signal disables gate K77. Simultaneously from the $\overline{Ru}$ output of the inverter a logic 1 signal enables gates K189, K191, K192 and K195. From the $\overline{Ru}$ output of inverter N23 a logic 0 signal disables the operation of gates K188, K190 and K193. From the output of gate K77 a logic 1 signal is fed to the input of gate D10 and ensures the working order of the memorising circuit until the F1 input of gate K77 enters a logic 1 signal (I.E. until flip-flop F1 is set in running order).

The following pulse S1 through gate K195 and the differentiating circuit sets flip-flop Z16 and starts the reverse counting of the Z counter. During reverse counting of the Z counter occurs the re-writing and shift of the number in the MR register to the right by one byte.

From output of flip-flop Z16 a logic 1 signal disables gate K196. From output S16 of inverter N87 a logic 1 signal enables gate K81. After the readout of the four bits of information (0000) of the 16th byte, pulse S1 through gate K74 and the differentiating circuit sets flip-flop LES-SCHREIB into working the order.

From output SCHREIB a logic 1 signal disables gate K81, from the output of which a logic 1 signal through gate D11 is fed to the input of inverter N29. From output MRS of the inverter a logic 0 signal disables the operation of gate K6 preventing the writing of the X12 marker into the 16th byte of the MR register. Pulse VLS of the 16th byte through gate K187 and the differentiating chain ensures the setting of flip-flops Z1, Z2, Z4 and Z8 into the working order and so switches on counter Z. The position of the Z counter corresponds to control of the following, I.E. by the 15th, byte. Simultaneously pulse VLS through the differentiating circuit set flip-flops E4 and E8 into the initial state. From outputs E4 of the flip-flops E4 and E8 and from inverter N21 a logic 0 signal disables gate K56. As a result at the $\overline{X}$, X. Outputs of inverters N17 and N18 the signals change to the initial state. Re-writing and shift of the information of the four bits of the remaining bytes of the MR register and the X10 marker occurs in the usual sequence.

During the readout of the four bits of the 4th byte the X10 marker is rewritten into the four flip-flops of register A. From the outputs of flip-flops A2 and A8 a logic 1 signal disables gate K57, from the output of which a logic 1 signal through gate D5 is fed to the input of inverter N17. From output X of the series-connected inverter N18 a logic 1 signal enables gate K158. Pulse VLS of the 4th byte through gate K158 and the differentiating circuit resets flip-flop VER into the initial state. Simultaneously pulse VLS ensures the re-writing of the X10 marker from the four flip-flops of register A into the four flip-flops of register E and switching the Z counter for re-writing without shift of the remaining three bytes of the MR register. Clock pulses S during the readout of the 3rd byte consecutively through gates K60 and K70 reset flip-flops E2 and E8 into the initial state. As a result of this the X10 marker is not written into 3rd the byte of the MR register. Flip-flop Z16 remains set after the reading and writing of the 1st byte. From output Z16 of the flip-flop a logic 1 signal disables gate K196. From output S16 of inverter N87 a logic 1 signal disables gate K150. (The controlling VER input of the differentiating circuit of flip-flop F1 enters a logic 0 signal). Pulse VLS of the 16th byte ensures the setting of flip-flops Z1, Z2, Z4 and Z8 and control of the 15th byte of the MR register. From outputs $\overline{Z1}$, $\overline{Z2}$, $\overline{Z4}$ and $\overline{Z8}$ logic 0 signals disable gate K196. A positive voltage drop from the S16 output of inverter N87 through gate K150 and the differentiating circuit resets flip-flop F1 into the initial state. From output F1 of inverter N63 a logic 0 signal disables gate K77. The memorising circuit is switched into the initial state, at outputs Rü and $\overline{R\ddot{u}}$ of inverters N23 and N24 are restored the initial signals, which ensure further operation of the Z counter in the forward direction.

Pulse VLS of the 15th byte through gate K187 and the differentiating circuit ensures the sequential reset of flip-flops Z1, Z2, Z4 and Z8 into the initial state.

Flip-flop Z16 remains in running order. At output $\overline{S16}$ of inverter N88 a logic 0 signal is generated. Pulse VLS of the 16th byte through the differentiating circuit with $\overline{S16}=0$ resets flip-flop Z16 into the initial state and turns off the Z counter. After the disconnection of the Z counter in the four planes of the MR register the number 0000000000763542 will be stored.

(0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0111 0110 0011 0101 0100 0010)

Sequential pulse S1 through gate K186 sets flip-flop Z1 into the working order and starts the Z counter, whose operation ensures the display of the written information in the four planes of ferrite cores of the MR register.

III.2.3. Entry of a number with less digits than the Decimal Point setting.

The entry of digits of the entire and fractional part of a number occurs in a sequence, analogous to the description of the example of the entry of the number 763,542.

After the end of the entry of a number with a quantity decimal digits less than the established degree of accuracy, which let us take as equal to three decimal points (10^{-3}), the decimal point is included by entering one of the functional keys for the completion of the specific operation. The operation of a key ensures the shift of the number and the combination of its bytes in accordance with the degree of accuracy of the forthcoming calculations accepted. The closed contact of the pressed key through one or several diodes of the functional keyboard encoder (Fig. 19) connects a logic 0 signal to the input of keyboard filter L25. From output FU0 of the diagram a logic 0 signal enters the controlled input and prepares for the operation the differentiating circuit of flip-flop VOR.

Pulse EING through the differentiating circuit sets flip-flop VOR into the working order. A positive voltage drop of the $\overline{VOR}$ output of inverter N59 through the differentiating circuit sets flip-flop VER into the working order.

After switching of the contact of the entered functional key into its initial state, at the ST+KO output of inverter N61 a logic 1 signal is generated, which enables gate K186.

Pulse S1 through gate K186 and the differentiating circuit sets flip-flop Z1 incrementing the Z counter. During the first cycle of the Z counter the number, established in the MR register together with the X12 and X10 markers are shifted one byte to the left.

From output $\overline{VOR}$ of inverter N59 a logic 0 signal disables the operation of gate K160 of the inversion of the VER flip-flop into the initial state.

If as a result of the first shift the X12 marker is not read from the 4 bits of the 16th byte of the MR register, counter Z is included for the following error and the shift of the number (quantity of operations of shift it is determined by the position of the decimal point switch).

The shift of the number in the MR register occurs until the X12 marker is found from the 16th byte of the MR register. After reading out of the X12 marker in the usual sequence occurs the shift of the number in the opposite direction, the erasure of the X10 marker, the resetting of flip-flops VER and F1 into the initial state and stopping the Z counter. As a result of stopping the Z counter at the $\overline{Z}$ output of inverter N36 a logic 1 signal is generated enabling the operation of gate K151.

Clock pulse S through gate K151 and the differentiating circuit resets flip-flop F3 into the initial state. Flip-flop VOR remains set and ensures preparation for the operation of the corresponding functional key.

As an example of the automatic combination of bytes, the number 763,5 which was entered before the operation of a functional key, the number $0X_{12}000000000763X_{10}5$ was stored into the four planes of the MR register in the following order:

(0000 1100 0000 0000 0000 0000 0000 0000 0000 0000 0000 0111 0110 0011 1010 0101)

After the operation of a functional key and the corresponding shifts of the number, in the four planes of the MR register will be stored 0000000000763500 in the following order:

(0000 0000 0000 0000 0000 0000 0000 000 0000 0000 0111 0110 0011 0101 0000 0000)

In the case, when a quantity of the decimal digits of the number corresponds to the established degree of accuracy of calculations, after the operation of a function key, automatic shift is not included. The flip-flop VER is set into the working order from a positive voltage drop, entered from the $\overline{VOR}$ output of inverter N59. Sequential clock pulses S through gate K151 and the differentiating circuits with $\overline{VOR}=0$ reset flip-flops F3 and VER into the initial state. Gate K151 is prepared for the operation by the initial state of flip-flop F1 and the Z counter.

III.2.4. Entry of "minus" sign.

A negative number sign "minus" is written as a code 0001 in the 16th byte of the MR register with the operation of the "-# " key, the closed contact of the pressed key through the encoder diodes connects a logic 0 signal to the inputs of the keyboard functional encoder filters L17, L23 and L25. From output FU0 of the keyboard filter L25 a logic 0 signal simultaneously is fed to the input of flip-flop ST and the controlling input of the differentiating circuit of the VOR flip-flop.

From output SUB0 of the keyboard functional encoder filter L23 a logic 0 signal enables the operation the differentiating circuit of the MZ flip-flop. Pulse EING by a positive voltage drop set flip-flops VOR, F6, VER and MZ into the working order. A positive voltage drop of the $\overline{VER}$ output of inverter N67 on the collector input resets and blocks flip-flop UV in running order.

After resolution of a question of the shift of the number into correspondence with the description of the operation of diagram (Section. III.2.3) flip-flops F3, VER and UV reset into the initial state. From output F3 of inverter N65 a logic 0 signal through gate D24 is fed to the input of inverter N51.

From the EING2 output of the inverter a logic 1 signal enters the input resistor of gate K141. After setting flip-flop ST into the working order at output ST+K0 of inverter N61 a logic 1 signal is generated, which enables gate K186. Pulse S1 through gate K186 and the differentiation chain sets flip-flop Z1 incrementing the Z counter. The operation of the Z counter occurs simultaneously with the arrival a logic 1 signal at output EING2 of inverter N51. After disconnecting (stopping ?) the Z counter, at output S16 of inverter N87 is formed a positive voltage drop, which through gate K141 and the differentiating circuit resets flip-flop R into initial state. From output K of inverter N58 a logic 1 signal enables gate K194. Simultaneously from output $\overline{Z}$ of inverter N36 a logic 1 signal disables gate K63. From the output of the gate a logic 1 signal is fed to the input of inverter N20. From output X + E8 of inverter N20 a logic 0 signal enters the control input and enables the operation the differentiation chain of flip-flop Z16. Pulse S1 through gates K194 and K142 simultaneously sets flip-flop Z16 into working, and reset flip-flops R and VOR into the initial state.

A positive voltage drop from output R of inverter N58 through the differentiation chain resets flip-flop F6 into the initial state.

The working order of the Z16 flip-flop corresponds to control of the 16th byte of the MR register.

From outputs S16, $\overline{R}$,and $\overline{VOR}$ of inverters N57, N59 and N87 logic 1 signals disable gate K152. From the output of gate K152 a logic 1 signal through gate D1 is fed to the input of inverter N4. From output C1 of the inverter a logic 0 signal disables the operation of gate K24 and the inhibit stage BL1 pulses. Read and write cycles produce the writing of the "minus" sign code 0001 into the four bits of the 16th byte of the MR register. Pulse VLS of the 16th byte through the differentiating circuit resets flip-flop Z16 into the initial state and turns off the Z counter. Flip-flop MZ resets into the initial state from a positive voltage drop on input EING or $\overline{VOR}$ of the differentiating chains with the operation respectively of a digital or functional key.

III.2.5. Erasing the MR register.

Clearing the MR register is accomplished by pressing the master clear key Lö or as a result of pressing a digital key after the completion of an arithmetic operation.

1. Clearing written information in the MR register with the Lö key is described in section III.1.

2. Clearing written information in the MR register with the clear entry key "C " flows in the following sequence, analogous to the description of the entry of the first digit of a number, with some changes which consist of the following.

After switching the key contact a logic 0 signal through the diodes of the digital keyboard encoder enters the keyboard filters L15 and L10. From outputs Z/0 and CO of the keyboard filters a logic 0 signal enters the control input differentiation chains of flip-flops F3, F1 and VER. In the usual sequence at the output of inverter N56 is formed the pulse train EING.

A positive voltage drop of pulse EING through the differentiating circuits sets flip-flop VER and resets flip-flops F3 and F1. From outputs VER and $\overline{F3}$ of inverters N68 and N64 logic 1 signals disable gate K86. From the output of gate K86 a logic 1 signal through gate D14 is fed to the input of inverter N34. At output HV of the inverter a logic 0 signal is generated, which disables the operation of the read amplifiers, inversion of flip-flop VER into the working order ensures the start of the Z counter through gate K186 and the completion of the shift operation without reverse record, I.E.. The erasure of information in the MR register. After erasure of the information in the 16th byte of the MR register The VLS pulse of the 16th byte through gate K160 and the differentiating circuit with ÜBER = 0 resets flip-flop VER into the initial state.

3. Erasure of the information in the MR register occurs if:

3a) After the operation of a digital key before the operation of the "comma" key flip-flop F3 is located in running order;

3b) After operation of the "comma" key flip-flops F1 and F3 are located in running order;

3c) After the completion of an arithmetic operation or re-writing flip-flops F1 and F3 will be in the initial state.

In all cases operation of the "C" key respectively ensures the resetting of flip-flops F1 and F3 into the initial state and setting of flip-flop VER into the working order. The inversion of flip-flops VER and F3 in the sequence, analogous to the description of the point of 2 these paragraphs, ensures the erasure of the MR register information.

III.2.6. Display of digital information markers and "minus" sign.

Fundamental device operation and the start in operating conditions of the display unit occurs in accordance with the description of sections III.8, III.1.1., III.1.3. After operation of relay REL1 the -UA, +UA voltage supplies are simultaneously connected to the anode and cathode amplifiers of the digital display lamps. Operational control of the numerical cathodes amplifiers is produced by signals A1-A8, $\overline{A1}$ - $\overline{A8}$ and C1-C8 through gates K53, K62, K5, K4, K3, K48, K47, K46, K45 and K44, which are configured as a decoder and ensure the transfer of the MR register digital information from the binary coded decimal numeration system into the decimal system (Fig. 30).

The amplifier outputs ZV0, ZV1, ZV2, ZV3, ZV4, ZV5, ZV6, ZV7, ZV8 and ZV9 are connected the cathodes of identical numbers (Fig. 31).

Operational control of the anode amplifiers is produced by signals Z1 - Z8 and $\overline{Z1} \div \overline{Z8}$ through gates K197 - K211. The amplifier outputs SV1 - SV15 are each connected to the anodes of the digital indicator lights.

Prior to the entry of any information and as a result of the erasure of the operational registers by the Lö key in each 4 bits of register MR is written 0000. Consequently, during the operation of the Z counter the read and write cycles do not cause a change in the initial state of the flip-flops of the A register. From outputs C1, C2, C4 and C8 of inverters N4, N6, N8 and N10 logic 1 signals enable gate K53
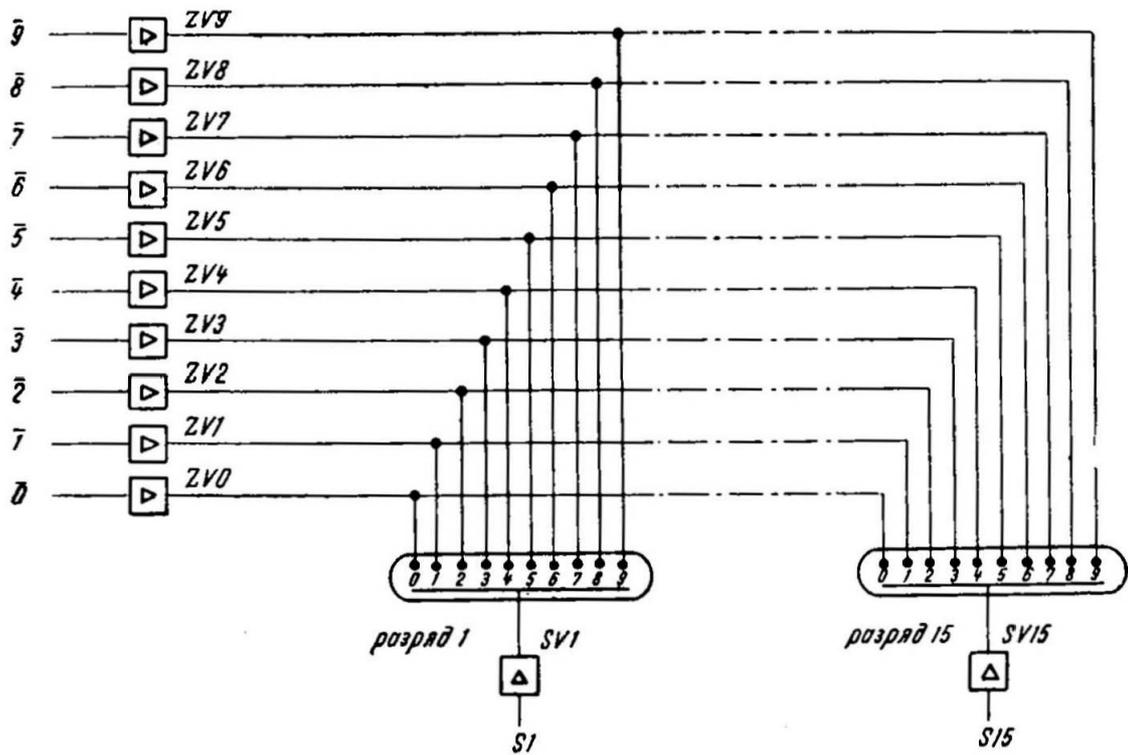
Fig. 31. Circuit diagram for connecting cathode amplifiers to the numerical cathodes of the display.

During the readout of each byte inputs U and LES enter logic 0 signals and disable gate K90. At the output AU of inverter N35 a logic 1 signal is generated disabling gate K53. From the output of gate K53 a logic 1 signal through gate D8 is fed to the input of inverter N16. From the ^{0} output of inverter N16 a logic 0 signal enables the cathode amplifier for the number 0. At the output of each amplifier the voltage -U$_A$ is generated which is connected to all of the cathodes of the display lamps for the number 0.

Operation of the Z counter through gates K197 - K211 enables the anode amplifiers. At each amplifier output a -U$_A$ voltage is generated, which is simultaneously connected to the anodes of the corresponding display lamps and with the -U$_A$ cathode voltage causes each number 0 to illuminate. The sequential operation of the Z counter ensures the number 0 illuminates in all positions of the display unit.

The relatively short time interval of one step of the Z counter in a comparatively frequent sequential connection of the feeding voltages does not cause any noticeable change in the illumination of the cathodes of each digital lamp.

After the entry of the first number of an example, through gate K186 the Z counter is incremented and the usual sequence of re-writing the information of the MR register → MR is carried out.

Inversion of flip-flop Z1 ensures control of the 1st byte of the MR register.

From output Z1 of inverter N79 a logic 1 signal disables gate K197. From the output of gate K197 a logic 1 signal enables the anode amplifier, and as a result the $+U_A$ voltage supply is connected to the anode of the 1st digital lamp of the display. Flip-flops UV and LES-SCHREIB are in the initial state. The first cycle of the readout produces a readout of the number 7 (0111) from the four ferrite core planes of the MR register into the flip-flops of the A register. Flip-flops A1, A2 and A4 are set into the working order, from inverters N5, N7 and N9 logic 1 signals enable gate K46. From the output of gate K46 a logic 1 signal is fed to the input of inverter N95. From the inverter output a logic 0 signal enables the cathode amplifier for the number 7 cathode. As a result voltage $-U_A$ is connected to all the number 7 cathodes of all the indicator lights.

The simultaneous connection of the operating voltage of $+U_A$ and $-U_A$ to the cathode and anode of the 1st indicator light ensures the illumination of the number 7 only in the 1st position of the display.

Pulse S1 through gate K74 and the differentiating circuit sets flip-flop LES-SCHREIB into the working order.

The first write cycle produces the re-writing of the number 7 into the four bits of the 1st byte of the MR register. The following S1 pulse through gate K74 and the differentiating circuit resets flip-flop LES-SCHREIB into the initial state. A positive voltage drop from output SCHREIB of inverter N26 through the differentiating circuit sets flip-flop UV into the working order. From output V of inverter N28 a logic 1 signal disables gate K85. From the output of gate K85 a logic 1 signal enters through gate D14 to the input of inverter N34. At output HV of the inverter a logic 0 signal is generated, blocking the operation of the read amplifiers.

The second read cycle erases the information in the four ferrite core planes of the 1st byte of the MR register. Pulse S1 through gate K74 and the differentiating circuit sets flip-flop LES-SCHREIB into the working order.

The second write cycle writes the number 7 (0111) into the four ferrite core planes of the 1st byte of the MR register.

Pulse S1 following through gate K74 and the differentiating circuit resets flip-flop LES-SCHREIB into the initial state. A positive voltage drop of the SCHREIB output of inverter N26 through the differentiating circuit resets flip-flop UV into the initial state.

At the output of inverter N33 is generated the VLS pulse of the first byte, which through gate K187, and differentiating circuits temporarily reset flip-flops A1, A2, A4, Z1 into the initial state.

From output V of inverter N28 a logic 0 signal disables gate K85. The resetting of flip-flop Z1 into the initial state switches the Z counter for control and displays the 2nd digit of the MR register.

Digital lamps of the 2nd - 15th digits of the display produce a display of the 0 number from the Z counter. Display of the written digital information in the MR register occurs prior to the entry of the second number of an example. After the entry of the second and subsequent numbers of an example the display occurs analogously.

The display of the X12 marker is produced with the working order of flip-flops A4 and A8. From outputs A4 and A8 of inverters N9 and N11 logic 1 signals disable gate K56. From output X of inverter N18 a logic 1 signal through the gate D8 is fed to the input of inverter N16. From the output of inverter N16 a logic 0 signal enables the cathode amplifier, which ensures the display of the number 0.

Display of the X10 marker is produced with the working order of flip-flops A2 and A8. From outputs A2 and A8 of inverters N7 and N11 logic 1 signals enter the inputs and disables gates K57 and (K51)* K56. From output X of inverter N18 a logic 1 signal through gate D8 is fed to the input of inverter N16. From the output of the inverter a logic 0 signal enables the cathode amplifier, which ensures the display of the number 0.

Simultaneously from the output of gate (K51)* K56 a logic 1 signal through gate D6 is fed to the input of inverter N89. From the output of the inverter a logic 0 signal enables the cathode amplifier, which ensures the display of the number 1, as a result the display of the X10 marker is produced by the combination numbers 0 and 1.

The display of "minus" sign occurs as a result of reading and writing in the 16th byte of the MR register.

The first read pulse produces re-writing of the "minus" sign code 0001 into the four flip-flops of register A. From output A1 of inverter N5 a logic 1 signal prepares for the work gate K157. Pulse VLS of the 16th byte through the differentiating circuits reset flip-flops A1 and Z16 into the initial state. A positive voltage drop from output A1 of inverter N5 through gate K157 and the differentiating circuit sets flip-flop MZ into the working order.

From output MZ of the flip-flop a logic 1 signal is fed to the input of the amplifier V700. From the output of the signal amplifier a logic 0 level through the 82 ohm resistor ensures the illumination of the miniature incandescent lamp of the "minus" sign display (Fig.26).

During the Z counter cycle there follows in the sequence, analogous to the description, through gate K157 the flip-flop MZ resets into the initial state. After each cycle of the Z counter flip-flop MZ inverts into the working or initial condition.

The comparatively short time interval of one cycle of the Z counter and the frequent connection of the signal voltage does not cause any noticeable changes in the illumination of the "minus " sign indicator.

* Note - The gate K56 listed here is a correction from the original Russian manual which listed the gate as K51, this did not match the circuit and original GDR logic drawings.

III.3. Algebraic Addition.

An algebraic Addition operation is carried out with the operation of the functional keys "+", "- ", "+ I", "+ II", "+ III", "–I", "–II" and "–III".

The operation occurs between the MR register and a corresponding AC register with the result of the operation in AC register.

Depending on the functional key used (Addition or Subtraction), the signs and the absolute values of the terms the machines arithmetic-logic unit performs an Addition or Subtraction arithmetic operation in accordance with the given table:

Switched Key	Sign and value of register	Operation carried out	Sign of result with AC>MR AC<MR	
"+"	(+AC) + (+MR)	Addition	+	+
"+"	(-AC) + (-MR)	"	-	-
"+"	(+AC) + (-MR)	Subtraction	+	-
"+"	(-AC) + (+MR)	"	-	+
"-"	(+AC) - (+MR)	"	+	-
"-"	(-AC) - (-MR)	"	-	+
"-"	(+AC) - (-MR)	Addition	+	+
"-"	(-AC) - (+MR)	"	-	-

Operational control of the AC register with the completion of the algebraic addition operation occurs depending on the functional key used "+", "-", "±I", "±II " and "±III ".

III.3.1. Operational control of the AC0 register.

With the operation of a "plus" or "minus" key a logic 0 signal through the switched contact and diodes of the functional keyboard encoder are fed to the inputs of the keyboard filter circuits L22 and L24. From the filter outputs ADD0, (±)0 logic 0 signals enter the controlling inputs of the differentiating circuits of flip-flops B1 and F2. A positive voltage drop of pulse EING through the differentiating chain set flip-flops B1 and F2 into the working order. When V = 1 gate K117 is enabled. From the output of gate K117 a logic 1 signal enters through gate D21 to the input of inverter N43. From the output of the inverter a logic 0 signal is fed to the input of gate D22. Gate K126 is enabled. From the output of gate K126 a logic 1 signal enters through gate D23 to the input of inverter N44. At output AC of the inverter a logic 0 signal is generated, which disables gate K127. From the output of gate K127 a logic 0 signal is fed to the input of gate D22. The remaining inputs of gate D22 at this time also enter logic 0 signals. At output of the gate a logic 0 signal is generated, which is fed to the input of inverter N45. From output AC0 of the inverter a logic 1 signal enters gate K8 and ensures operational control of the AC0 register.

III.3.2. Operational control of the AC1 register.

With the operation of a "+ I" or "- I" key a logic 0 signal through the switched contact and diodes of the functional keyboard encoder are fed to the inputs of the keyboard filter circuits L18 and L24. From the filter outputs (I)0 and ADD0 logic 0 signals enter the controlling inputs of the differentiating circuits of flip-flops B1 and F4.

A positive voltage drop of pulse EING enters the inputs of the differentiating chains and set flip-flops B1 and F4 into the working order.

From output $\overline{F4}$ of inverter N72 a logic 0 signal enters the input and disables gate K126. When the V = 1 gate K117 is enabled. Consequently, from the output of inverter N43 a logic 0 signal is fed to the input of gate D23. The remaining inputs of gate D23 at this time also enter logic 0 signals. From the output of gate D23 a logic 0 signal is fed to the input of inverter N44, at output AC0 of the inverter a logic 1 signal is generated, which disables gate K127. From the output of gate K127 a logic 1 signal enters through gate D22 to the input of inverter N45. At the output of the inverter a logic 0 signal is generated, which enters the input and disables the operation of gate K8 for the administration of the AC0 register. Simultaneously from output AC of inverter N44 a logic 1 signal enables gates K9, K10 and K11. From the outputs of inverters F4 and $\overline{F5}$ logic 1 signals enters gate K9 where it ensures operational control of register AC1.

III.3.3. Operational control of the AC2 register.

Operational control of register AC2 occurs in a sequence, analogous to the description "Operational control of the AC1 register".

With the operation of a "+ II" or "- II" key instead of the keyboard filter circuit L18 the keyboard filter circuit L19 is used. Consequently, instead of flip-flop F4 inverting into the working order flip-flop F5 is inverted.

From outputs $\overline{F4}$ and F5 of inverters N72 and N75 logic 1 signals are fed to the inputs of gate K10 and ensure the operational control of the AC2 register.

III.3.4. Operational control of the AC3 register.

Operational control of register AC3 occurs in a sequence, analogous to description "Operational control of the AC1 register".

With the operation of a "+ III" or "- III" key at outputs (I)0 and (II)0 of the keyboard filter circuits L18 and, L19 we obtain a logic 0 signals. As a result flip-flops F4 and F5 invert into the working order. From outputs F4 and F5 of inverters N73 and N75 logic 1 signals are fed to the inputs of gate K11 and ensure the operational control of the AC3 register.

III.3.5. Analysis of the signs of the terms.

In the description sequence in section III.2.3 preparation occurs for the completion of the algebraic Addition operation, I.E. The shift and entry of the number in accordance with the assigned calculations degree of accuracy. After the end of the preparatory part of the operation in the usual sequence through gate K186 the Z counter is indexed, which ensures re-writing the information of the MR register → MR and display of the term. During the Z counter cycle from output EING2 of inverter N51 a logic 1 signal enters the control input and prepares for the work of gate K141. After the setting of flip-flop Z16 into the working order from output S16 of inverter N87 a logic 1 signal disables gate K141. The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16} = 0$ resets flip-flop Z16 into the initial state and turns off the Z counter. A positive voltage drop from output S16 of inverter N87 through gate K141 and the differentiating circuit sets flip-flop R into the working order. From output R of inverter N58 a logic 1 signal enables gates K117 and K194. Simultaneously from output $\overline{R}$ of the inverter N57 a logic 0 signal disables the operation of gate K186. Sequential pulse S1 through gate K194 and the differentiating chains simultaneously set flip-flops Z16 into the working state (with Z+E8 = 0) and resets VOR into the initial state. Consequently, the preparatory part of the algebraic Addition operation flows equally with the entry of any of the functional keys.

The end of the preparatory part of the operation coincides with the beginning of the analysis of the signs of the terms, which occurs between register MR and the corresponding AC register. Depending on the result of the signs analysis the arithmetic-logic unit performs an Addition or Subtraction operation.

The operation of Addition is carried out with the condition of the initial state of flip-flop MZ, I.E., when at outputs ADD1 and ADD (addition) of inverters N46 and N48 where logic 1 signals are generated.

When as a result of the analysis of the signs of the terms flip-flop MZ remains set and at output SUB (Subtraction) of inverter N47, a logic 1 signal is generated, and the arithmetic-logic unit performs a Subtraction operation.

With the operation of an Addition key "plus" the analysis of the signs of the terms is carried out in the following order.

From the outputs of gates D11 and D15 with U=1, logic 0 signals are fed to the inputs of inverters N29 and N38. At outputs MRS of inverters N29 and N38 a logic 1 signal is generated, which enters gate K6 and ensures control of the MR register.

From the output of gate K126 a logic 1 signal through gate D23 is fed to the input of inverter N44. From output AC of the inverter a logic 0 signal disables the operation of gate K127. The gate K117 with V=1 is enabled. From the output of gate K117 a logic 1 signal enters through the gate D21 to the input of inverter N43. From the output of the inverter a logic 0 signal is fed to the input of gate D22.

Simultaneously the remaining inputs of gate D22 also enter logic 0 signals. Consequently, during the working order of flip-flop UV to the input of inverter N45 from the output of gate D22 a logic 0 signal is input. At output AC0 of the inverter a logic 1 signal is generated, which ensures control of the AC0 register. The working order of flip-flop Z16 determines control of the sign digit of the number.

A)   Analysis of signs when the Add key is pressed.

1.   (-MR) + (-AC0).

Flip-flop UV is in the initial state, at output U of inverter N27 a logic 1 signal generated.

The first read cycle reads the "minus" sign code 0001 of the four bits of the 16th byte of the MR register into the four bits of the A register.

The first write cycle rewrites the "minus" sign code 0001 of the four flip-flops of register A into the four ferrite core planes of the 16th byte of the MR register.

A positive voltage drop of the SCHREIB output of inverter N26 through the differentiating circuit sets flip-flop UV into the working order. A positive voltage drop of the output of inverter N27 through gate K132 and the differentiating circuit with F3 = 0 resets flip-flop A1 into the initial state. A positive voltage drop of the A1 output of inverter N5 through gate K157 and the differentiating circuit sets flip-flop MZ into the working order. Simultaneously a positive voltage drop of the A1F output through the differentiating circuit with SUB = 0 sets flip-flop E1 into the working order. Sequential clock pulses S through gate K50 and the differentiating circuit with VER = 0 resets flip-flop E1 into the initial state. From output E1 of the flip-flop a logic 0 signal disables gate K34. Gate K98 is enabled. From the output of inverter N39 a logic 0 signal through the diode on the collector input disables the operation of the A2 flip-flop. As a result a positive voltage drop at the output of gate K34 through the differentiating chain does not set flip-flop A2 into the working order. After setting the UV flip-flop into the working order from the output V of inverter N28, a logic 1 signal through gates K117 and D21 is fed to the input of inverter N43. From the output of inverter N43 a logic 0 signal through gate D22 is fed to the input of inverter N45. At output AC0 of the inverter a logic 1 signal is generated, which ensures control of the AC0 register.

Simultaneously from output AC0 of inverter N45 a logic 1 signal through gate D11 is fed to the input of inverter N29. From output MRS of inverters N29 and N38 a logic 0 signal enters gate K6 and disables the operation of the MR register.

The second read cycle reads the "minus" sign code 0001 from the four ferrite core bits of the 16th byte of the AC0 register into the four flip-flops of register A.

The second write cycle rewrites the "minus" sign code 0001 of the four register A flip-flops into the four ferrite core bits of the 16th byte of the AC0 register.

A positive voltage drop of the SCHREIB output of inverter N26 through the differentiating circuit resets flip-flop UV into the initial state.

During the second write cycle the VLS pulse through the differentiating circuit resets flip-flop A1 into the initial state.

Positive voltage drop of the output A1 of inverter N5 through gate K157 and the differentiating circuit resets flip-flop MZ into the initial state.

Simultaneously a positive voltage drop of the A1F output through the differentiating circuit with SUB = 0 sets the E1 flip-flop into the working order. Sequential clock pulses S through gate K50 and the differentiating circuit with VER = 0 resets flip-flop E1 into the initial state.

Pulse VLS through the differentiating circuit resets flip-flop Z16 into the initial state and turns off the Z counter.

A positive voltage drop of the Z16 output of the flip-flop through the differentiating circuit sets flip-flop F3 into the working order. From output F3 of inverter N65 a logic 1 signal enters the control input of the differentiating circuit disabling the operation of gate K132. From output F3 of inverter N64 a logic 0 signal disables the operation of gates K98 and K157. Simultaneously from output Z16 of the flip-flop a logic 0 signal disables gate K196. A positive voltage drop from output S16 of inverter N87 through gate K183 and the differentiating circuit with F1 = 0 sets flip-flop Z1 incrementing the Z counter. From output $\overline{S16}$ of inverter N88 a logic 1 signal enables gate K111. The initial state of the MZ flip-flop disables the operation of gate K111.

From the output of gate K111 a logic 0 signal passes through gate D19 to the input of inverter N46. At outputs of inverters N46, N48, ADD1 and, ADD logic 1 signals are generated.

2.   (+MR) + (+AC0).

During readout and the record in the 16th byte of registers MR and AC0 occurs the re-writing of the "plus" sign code 0000, as a result of which flip-flops A1 and MZ remain in the initial state. Consequently, after the end of the signs of terms analysis at outputs ADD1 and ADD of inverters N46 and N48 logic 1 signals are generated.

3.   (-MR) + (+AC0).

The first read-write cycles correspond completely to the description of reading and writing of the "minus" sign code 0001 in the MR registers MR in example 1. As a result of the first read and write cycle the MR flip-flop is located in running order.

During the second read and write cycle in the AC0 register occurs the re-writing of the positive "plus" sign code 0000, as a result of which the A1 flip-flop remains in the initial state, and flip-flop MZ - in the working.

After inversion of the flip-flop Z16 into the initial state in the sequence of example 1 occurs switching of the Z counter. From output $\overline{S16}$ of inverter N88 a logic 1 signal disables gate K111.

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At the output of gate K111 a logic 1 signal is generated, which through gate D19 is fed to the input of inverter N46. From the ADD1 output of inverter N46 a logic 0 signal through gate D20 is fed to the input of inverter N47. At the SUB output of the inverter a logic 1 signal is generated.

4.   (+MR) + (-AC0).

During the first read and write cycle of the MR register there occurs the re-writing of the positive "plus" sign code 0000, as a result of which flip-flops A1 and MR remain in the initial state.

The second read and write cycle corresponds completely to the description of the read and write cycle of the "minus" sign code 0001 in the AC0 registers in example 1. As a result of the second read and write cycle flip-flop MR is located in running order. At the SUB output of inverter N47 a logic 1 signal is generated.

B)   Analysis of signs when the Subtract key is pressed.

After switching the contact of one of the Subtraction keys, through the functional keyboard encoder diodes a logic 0 signal is fed to the input of keyboard filter L23. From the SUB0 output of the keyboard filter a logic 0 signal enters the control input and enables the differentiating circuit of the MZ flip-flop. A positive voltage drop of the EING pulse through the differentiating circuit with SUB0 = 0 sets flip-flop MZ into the working order, which preliminarily determines the completion of the Subtraction operation.

5.   (+MR) - (+AC0).

Analogous with the description of example 2 during the read and write in the 16th byte of the MR and AC0 registers occurs the re-writing of the positive "plus" sign code 0000, as a result of which flip-flops A1 and MR are not switched. Consequently, after the end of the analysis of signs of the terms flip-flop MZ remains in running order. At the SUB output of inverter N47 a logic 1 signal is generated.

6.   (-MR) - (-AC0).

Flip-flop MZ is set prior to the beginning of the analysis of signs. The switching of flip-flops A1 and MZ occurs in a sequence, analogous to the description of the analysis of signs in example 1. Flip-flop MZ is switched twice and remains in running order during the analysis of signs. At the SUB output of inverter N47 a logic 1 signal is generated .

7.   (-MR) - (+AC0).

Switching of flip-flops A1 and MZ occurs in a sequence, analogous to the description of the analysis of the signs in example 3. During the analysis of signs the preliminarily established flip-flop MZ is switched from the working order into the reset state. In the initial state of flip-flop MZ at outputs ADD1 and ADD of inverters N46 and N48 logic 1 signals are generated.

8.   (+MR) - (-AC0).

Switching of flip-flops A1 and MR occurs in a sequence, analogous to the description of the analysis of the signs in example 4. During the analysis of signs the preliminarily established flip-flop MZ is switched from the working into the initial state. In the initial state flip-flop MZ at outputs ADD1 and ADD of inverters N46 and N48 logic 1 signals are generated.

Consequently, after the analysis of the signs in examples 1, 2, 7, 8 flip-flop MZ remains in the initial state. At the ADD1 and ADD outputs of inverters N46 and N48 logic 1 signals are generated, which determine completion by the arithmetic-logic unit of the Addition operation.

Flip-flop MZ remains in running order after the analysis of the signs in examples 3, 4, 5 and 6. At output SUB of inverter N47 a logic 1 signal is generated, which determines completion by the arithmetic-logic unit of the Subtraction operation.

III.3.6. Addition.

Based upon Addition of the numbers in the example below let us examine the sequence of operation:

$$
\begin{array}{r}
\text{MR} +\ \ 71 \\
+ \qquad\qquad\qquad \\
\underline{\text{AC0} +\ \ 65} \\
\text{AC0} + 136
\end{array}
$$

After the analysis of the signs of the terms flip-flops B1, F3, R and, Z1 are located in the working order, and MZ in the initial state. At outputs ADD1 and ADD of inverters N46 and N48 logic 1 signals are generated, which using the arithmetic-logic unit completes the addition operation. The position of the Z counter determines control of the 1st byte. At the output of gates D11 and D15 with U = 1 logic 0 signals are generated, which are fed to the inputs of inverters N29 and N38. From the MRS outputs of the inverters a logic 1 signal enters the input and prepares gate K6 for the administration of the MR register.

Flip-flops UV and LES-SCHREIB will be in the initial state. From outputs U and LES of inverters N25 and N27 logic 1 signals are generated, which accomplish the first read cycle.

The first read cycle reads the number 1 (0001) from the four ferrite core planes of the 1st byte of the MR register ferrite cores into the four bits of the A register. Flip-flop A1 sets into the working order. At the A1F output of the flip-flop a logic 1 signal is generated, which is fed to the input of the differentiating circuit of flip-flop E1. Pulse S1 through gate K74 sets flip-flop LES-SCHREIB into the working order. At outputs U and SCHREIB of inverters N26 and N27 logic 1 signals are generated, which enables the first write cycle.

The first write cycle rewrites the number 1 (0001) from the four flip-flops of register A into the four ferrite core planes of the 1st byte of the MR register. Pulse S1 through gate K74 resets flip-flop LES-SCHREIB into the initial state. A positive voltage drop at the SCHREIB output of inverter N26 through the differentiating circuit sets flip-flop UV into the working order. From the V output of inverter N28 a logic 1 signal enables gate K117. From the output of gate K117 a logic 1 signal enters through gate D21 to the input of inverter N43.

From the output of inverter N43 a logic 0 signal enters gate D22. The remaining inputs of gate D22 enter logic 0 signals. From the output of gate D22 a logic 0 signal is fed to the input of inverter N45. At the AC0 output of the inverter a logic 1 signal is generated, which enables gate K8 and ensures control of the AC0 register. Simultaneously from the AC0 output of inverter N45 a logic 1 signal through gate D11 is fed to the input of inverter N29. From the MRS output of the inverter a logic 0 signal enters the input and disables the operation of gate K6 and control of the MR register.

On the V and LES outputs of inverters N25 and N28 logic 1 signals are generated, which enables the second read cycle.

During the second read cycle the number 5 (0101) is read from the four bits of the 1st byte of the AC0 register ferrite cores into the four bits of the A register is accomplished. Flip-flop A1 resets into the initial state, and sets A4 into the working order. A positive voltage drop from the A1F output of flip-flop A1 through the differentiating circuit with SUB = 0 sets flip-flop E1 into the working order.

From output E1 of the flip-flop a logic 1 signal disables gate K34. Sequential clock pulses S through gate K50 and the differentiating circuit with VER = 0 resets flip-flop E1 into the initial state. From output E1 of the flip-flop a logic 0 signal enables gate K34. A positive voltage drop from the output of gate K34 through the differentiating circuit set flip-flop A2 into working order.

The working order of flip-flops A2 and A4 corresponds to writing the number 6 (0110), I.E.. To the sum of the terms of the first bytes of registers MR and AC0 into the flip-flops of the A register.

The following pulse S1 through gate K74 sets flip-flop LES-SCHREIB into the working order. On the V and SCHREIB outputs of inverters N26 and N28 logic 1 signals are generated, which enables the second write cycle.

During the second write cycle the re-writing of the number 6 (0110) from the four flip-flops of register A into the four ferrite core planes of the 1st byte of the AC0 register accomplished.

Pulse VLS of the 1st byte through the differentiating circuits reset flip-flops A2 and A4 into the initial state. Positive voltage drops in the A2F and A4F outputs through the differentiating circuits with SUB = 0 set flip-flops E2 and E4 into the working order. Simultaneously the VLS pulse through gate K187 switches the Z counter for control of the following, I.E. The 2nd, byte. Pulse S1 through gate K74 and the differentiating circuit resets flip-flop LES-SCHREIB into the initial state. A positive voltage drop from the SCHREIB output of inverter N26 resets flip-flop UV into the initial state. At outputs U and LES of inverters N25 and N27 logic 1 signals are generated, which accomplish the first read cycle. Sequential clock pulses S through gate K60 and the differentiating circuits with $\overline{E2} = 0$ and $\overline{E4} = 0$ reset flip-flops E2 and E4 into the initial state.

The read and write cycles of the 2nd byte are carried out in a sequence, analogous to the description of the 1st byte.

During the first read cycle the number 7 (0111) is read from the four bits of the 2nd byte of the MR register ferrite cores into the four flip-flops of register A. Flip-flops A1, A2, A4 invert into the working order. From outputs A1F, A2F and A4F logic 1 signals are fed to the inputs of the differentiating circuits of register E flip-flops E1, E2 and, E4.

During the first write cycle the re-writing of the number 7 (0111) from the four flip-flops of register A into the four ferrite core planes of the 2nd byte of the MR register occurs.

During the second read cycle the number 6 (0110) is stored from the four ferrite core planes of the 2nd byte of the AC0 register into the four flip-flops of register A. As a result of the readout flip-flops A2 an A4 invert into the initial state.

A positive voltage drop from the A2F and A4F outputs of the flip-flops through differentiating circuits with SUB = 0 set flip-flops E2 and E4 into the working order. From the outputs of flip-flops E2 and E4 logic 1 signals enter the inputs and disables gates K38 and K42.

Sequential clock pulses S through gate K60 and the differentiating circuits when $\overline{E2} = 0$ and $\overline{E4} = 0$ reset flip-flops E2 and E4 into the initial state. From outputs E2 and E4 of the flip-flops logic 0 signals enable gates K38 and K42. Positive voltage drops from the outputs of the gates through differentiating circuits set flip-flops A4 and A8 into the working order. From the A4 and A8 outputs of inverters N9 and N11 logic 1 signals enter the inputs and disable gate K56. From the output of gate K56 a logic 1 signal enters through gate D5 to the input of inverter N17. From output (X)* $\overline{X}$ of the inverter a logic 0 signal enters the input and disables gate K71. At the output of the gate a positive voltage drop, which sets flip-flop E8 into the working order, is formed through the differentiating circuit with U = 0. From output E8 of inverter N21 a logic 1 signal disables gate K64. Sequential clock pulses S through gate K70 and the differentiating circuit when K1 = 0 resets flip-flop E8 into the initial state. From output E8 of inverter N21 a logic 0 signal enables gate K64. A positive voltage drop from the output of gate K64 through the differentiating circuit with U = 0 sets flip-flop ÜBER into the working order.

A positive voltage drop from output $\overline{\text{ÜBER}}$ of the flip-flop through the differentiating circuit with $\overline{R} = 0$ set flip-flops E1 and E2 into the working order. From outputs E1 and E2 logic 1 signals enable the operation of gates K34 and K38. Sequential clock pulses S through gate K60 and the differentiating circuit with $\overline{E2} = 0$ resets flip-flop E2 into the initial state. From output E2 of the flip-flop a logic 0 signal enables gate K38. A positive voltage drop of the gate output through the differentiating circuit resets flip-flop A4 into the initial state. A positive voltage drop at A4F output of the flip-flop through the differentiating circuit with SUB = 0 sets flip-flop E4 into the working order.

From the output of flip-flop E4 a logic 1 signal disables gate K42. Sequential clock pulses S with a positive voltage drop through gates K50 and K60 and the differentiating circuits when $\overline{E4}$ = 0 and VER = 0 reset flip-flops E1 and E4 into the initial state. From outputs E1 and E4 logic 0 signals enter the inputs and shut gates K34 and K42. A positive voltage drop from the outputs of the gates through differentiating circuits set flip-flops A2 into the working order, and A8 into initial state. A positive voltage drop of the A8F output through a differentiating circuit with SUB = 0 sets flip-flop E8 into the working order. The following clock pulse S through gate K70 and the differentiating circuit with S1 = 0 resets flip-flop E8 into the initial state.

The second switching of the flip-flop E8 does not change the working order of flip-flop ÜBER.

During the transfer of the overflow bits from the four bits of the A register through the four flip-flops of the E register, gate K49 is in the disabled state. From the output of the gate a logic 0 signal is fed to the input of inverter N14. From output E of the inverter a logic 1 signal disables gate K166. From the output of gate K166 a logic 1 signal enters through gate D25 to the input of inverter N69. From output M of the inverter a logic 0 signal enters the input and disables the operation of gates K74 (read/write) and K162.

The closed state of gate K162 prevents the operation of the monostable shaping the t pulses, $\bar{t}$ creates the delay for the completion of the second write cycle.

As a result of executing the second read cycle and transfer of the overflow, flip-flops A1, A2 and ÜBER remain in running order, the working order of the flip-flops corresponds to the stored number 3 (0011) in register A flip-flops and also the unit of the transfer into the four bits of high-order digit, I.E. To the sum of the terms of byte.

After the setting of the four bit flip-flops of register E into the initial state the disabling of gates K74 and K162 is removed and in the usual sequence the second write cycle is carried out.

During completion of the second write cycle the re-writing of the number 3 (0011) from the four flip-flops of register A into the four ferrite core planes of the 2nd byte of the AC0 register occurs.

The resetting of the four bits of flip-flops of registers A and E in the initial state, switching of the Z counter and administration of the 3rd byte occurs in a sequence, analogous to the description of the resetting of four flip-flops of registers A and E into initial state and to switching the Z counter in the 1st byte.

In the four bits of the ferrite cores for the 3-15th bytes of registers MR and AC0 is written the number 0 (0000). Consequently, the first read and write cycles do not change the initial state of the four flip-flops of register A.

During the second read cycle at outputs LES, V, ÜBER of inverters N25, N28 and N22 logic 1 signals are generated, which disable gates K68 and K28. After the end of the read cycle the LES-SCHREIB flip-flop sets into the working order.

From the LES output of inverter N25 a logic 0 signal enables gate K68, at the output of the gate a positive voltage drop, which resets flip-flop ÜBER into the initial state, is formed through the differentiating circuit with U = 0. Simultaneously from output LES of inverter N25 a logic 0 signal enables gate K28. A positive voltage drop from the output of gate K28 through the differentiating circuit sets flip-flop A1 into the working order.

The second write cycle from the four flip-flops of register A rewrites the number 1 (0001) into the four bits of ferrite cores for the 3rd byte of the AC0 register. In accordance with the example the read and write cycles from the 4th through to the 15th bytes inclusively in the sequence, analogous to the description, carry out a step-by-step addition 0 (0000) + 0 (0000).

Pulse VLS of the 15th byte through gate K187 ensures the resetting of flip-flops Z1, Z2, Z4 and Z8 into the initial state. Flip-flop Z16 sets into the working order and ensures control of the 16th byte. From outputs $\overline{Z1}$, $\overline{Z2}$, $\overline{Z4}$ and $\overline{Z8}$ of inverters N78, N80, N82, N85 and the Z16 flip-flop logic 1 signals disable gate K196. From the output of gate K196 a logic 1 signal through inverters N86 and N87 enters the input S16 and disables gate $\overline{K212}$. From the output of the gate a logic 1 signal is fed to the input of inverter N88. From output $\overline{S16}$ of the inverter a logic 0 signal enters the differentiating input circuit of flip-flop Z16. Simultaneously from output Z8 of inverter N84 a logic 0 signal enables gate K140. At the output of the gate a positive voltage drop, which simultaneously resets flip-flop B1 into the initial state, is formed through the differentiating circuits setting F1 into the working order. From output F1 of inverter N63 a logic 1 signal enters the control input and disables the operation of the differentiating circuit of flip-flop Z1 with positive voltage drops on the output of gate K183. From output $\overline{B1}$ of inverter N49 a logic 1 signal disables gate K94. From the output of gate K94 a logic 1 signal enters through gate D15 to the input of inverter N38. At output MRS of the inverter a logic 0 signal is generated, which disables the operation of gate K6 and register MR. Consequently, the first read and write cycles do not re-writing the code of the sign of the number in the 16th byte of the MR register. As result of the operation the second read and write cycles in the usual sequence read and write the code of the sign of the number into the 16th byte of the AC0 register.

The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. The following S1 pulse through gates K142 and K194, and differentiating circuits with Z+E8 = 0 resets flip-flop R into the initial state, and sets Z16 into the working order.

From the K output of inverter N58 a logic 0 signal enables gate K94. As a result at the MRS outputs of inverters N29 and N38 a logic 1 signal is generated, which ensures control of the MR register.

A positive voltage drop from output R of inverter N58 through the differentiating circuit resets flip-flop F1 into the initial state. The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state. Pulse S1 through gate K186 and the differentiating circuit sets flip-flop Z1 into the working order which starts the Z counter, whose work ensures the display of the second term and sign of the number of 0000000000000071, written into the four ferrite core planes of the MR register.

0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0111 0001

As a result of completing the operation is obtained the sum of terms 136 and the sign of the numbers, which are written into the appropriate four bits of ferrite cores of the AC0 register.

0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0001 0011 0110

Flip-flop F2 remains in running order for the re-writing of the obtained sum from AC0 into MR.

III.3.7. Exceeding register length AC_n during Addition.

In the case, where the result of a sum exceeds the length of register AC_n, with the completion of the Addition operation the 15th byte flip-flop ÜBER sets into the working order. From the ÜBER output of inverter N22 a logic 1 signal enables the operation of gate K163. During incrementation of the Z counter the 16th byte flip-flop Z16 sets into the working order. From output Z16 of the flip-flop a logic 1 signal disables gate K196. From output S16 of inverter N87 a logic 1 signal disables gate K163. At the output of the gate a logic 1 signal is generated, which through gate D25 is fed to the input of inverter N69.

From output M of the inverter a logic 0 signal enters the inputs and disables the operation of gates K74 and K162.

The disabled state of gate K162 prevents the operation of the monostable, which blocks the completion of the read and write cycles and the operation of the Z counter. As a result of disabling the control gates of the anodes and cathodes amplifiers of the digital lamps are and turned off and the illumination of digital indicator lights ceases. Restoration of operating conditions for the arithmetic-logic unit circuit occurs after pressing the Lö key.

III.3.8. Subtraction with MR > AC0.

Based upon Subtraction of the numbers in the example below let us examine the sequence of operation:

$$
\begin{array}{r}
AC0 = \ -27 \\
+ \qquad\qquad \\
\underline{MR = +71} \\
AC0 = +44
\end{array}
$$

Flip-flops B1, F2, F3, R, Z1 and MZ are left in running order after the analysis of signs.

At the SUB output of inverter N47 a logic 1 signal is generated, which the arithmetic-logic unit uses to accomplish the Subtraction operation. The position of the Z counter ensures control of the 1st byte. From the output of gates D11 and D15 a logic 0 signal enters the inputs of inverters N29 and N38. From the MRS output of the inverters a logic 1 signal enables the operation of gate K6. Control of the MR register occurs with $U = 1$, control of the AC0 register is ensured through gate K117 with $V = 1$.

The first read cycle stores the number 1 (0001) from the four ferrite core planes of the 1st byte of the MR register into the four flip-flops of register A. Flip-flop A1 sets into the working order. From output A1F of the flip-flop a logic 1 signal through gates K29 and D1 is fed to the input of inverter N4. A positive voltage drop from output C1 of the inverter through the differentiating circuit with $ADD = 0$ sets flip-flop E1 into the working order. Sequential clock pulses S through gate K50 with $VER = 0$ resets flip-flop E1 into the initial state. Gate K34 is disabled with a logic 0 signal at output V.

The first write cycle rewrites the number 1 (0001) from the four flip-flops of register A into the four ferrite core planes of the 1st byte of the MR register.

The second read cycle stores the number 7 (0111) from the four ferrite core planes of the 1st byte of the AC0 register into the four flip-flops of register A. Flip-flop A1 resets into the initial state, flip-flops A2 and A4 are set into the working order. Positive voltage drops in the outputs C2 and C4 of inverters N6 and N8 through the differentiating circuits with $ADD = 0$ set flip-flops E2 and E4 into the working order. From outputs E2 and E4 of the flip-flops logic 1 signals disable gates K38 and K42. Sequential clock pulses S through gate K60 and the differentiating circuits with $\overline{E2} = 0$ and $\overline{E4} = 0$ reset flip-flops E2 and E4 into the initial state. From outputs E2 and E4 of the flip-flops logic 0 signals disable gates K38 and K42. Positive voltage drops on the outputs of the gates through the differentiating circuits resets flip-flop A4 into the initial state and sets A8 into the working order. A positive voltage drop from output C8 of inverter N10 through the differentiating circuit with $ADD = 0$ sets flip-flop E8 into the working order. From output E8 of the flip-flop a logic 1 signal disables gate K64.

Clock pulse S through gate K70 and the differentiating circuit with $S1 = 0$ resets flip-flop E8 into the initial state. From output E8 of inverter N21 a logic 0 signal enables gate K64. A positive voltage drop from the output of the gate through the differentiating circuit with $U=0$ sets flip-flop ÜBER into the working order. A positive voltage drop of the $\overline{UBER}$ output of inverter N22 through the differentiating circuit with $\overline{R} = 0$ set flip-flops E1 and E2 into the working order. From outputs E1 and E2 of inverters N13 and N15 logic 1 signals disable gates K34 and K38.

Sequential clock pulses S through gate K60 resets flip-flop E2 into the initial state. From output E2 of the flip-flop a logic 0 signal enables gate K38. A positive voltage drop from the output of the gate through the differentiating circuit sets flip-flop A4 into the working order. A positive voltage drop of the output C4 of inverter N8 through the differentiating circuit with ADD = 0 sets flip-flop E4 into the working order. The following clock pulse S through gates K50 and K60 reset flip-flops E1 and E4 into the initial state. From outputs E1 and E4 of inverter N13 and flip-flop logic 0 signals enter the inputs and shut gates K34 and K42. From the gate outputs a positive voltage drop through the differentiating circuits reset flip-flops A2 and A8 into the initial state.

The delay of the completion of the second write cycle occurs analogously with the description of delay during Addition.

The second write cycle stores the number 4 (0100) from the four flip-flops of register A into the four ferrite core planes of the 1st byte of the AC0 register.

The VLS pulse of the 1st byte resets flip-flop A4 into the initial state. Simultaneously a VLS pulse through gate K187 increments the counter for control of the following, I.E. by the 2nd byte.

The first read cycle stores the number 7 (0111) from the four ferrite core planes of the 2nd byte of the MR register into the four flip-flops of register A.

Flip-flops A1, A2, A4 invert into the working order. Positive voltage drops from the outputs C1, C2 and C4 of inverters N4, N6 and N8 through the differentiating circuits with ADD = 0 invert flip-flop E1, E2 and E4 into the working order. Sequential clock pulses S through gate K60 and the differentiating circuits with $\overline{E2}$ and $\overline{E4} = 0$ reset flip-flops E2 and E4 into the initial state. The following clock pulse S through gate K50 and the differentiating circuit with VER = 0 resets flip-flop E1 into the initial state.

The first write cycle rewrites the number 7 (0111) from the four flip-flops of register A into the four ferrite core planes of the 2nd byte of the MR register.

The second read cycle stores the number 2 (0010) from the four ferrite core planes of the 2nd byte of the AC0 register into the four flip-flops of register A. Flip-flop A2 resets into the initial state. A positive voltage drop of the output LES of inverter N25 through gates K28 and K68 reset flip-flops ÜBER and A1 into the initial state.

The second write cycle rewrites the number 4 (0100) from the four flip-flops of register A into the four ferrite core planes of the 2nd byte of the AC0 register.

In accordance with the examples, the read and write cycles from byte 3 through to the 15th byte inclusively carries out a step-by-step subtraction of 0 (0000) - 0 (0000).

The VLS pulse of the 15th byte in the usual sequence switches the Z counter for control of the following, 16th, byte. After inversion of the flip-flop Z16 into the working order from output $\overline{S16}$ of inverter N88 a logic 0 signal enables gate K111. At outputs ADD1 and ADD logic 1 signals are generated, and at output SUB - a logic 0 signal.

As a result the inversion of flip-flop Z8 into the initial state at output Z8 of inverter N84 is formed a positive voltage drop, which through gate K140 and the differentiating circuit with ÜBER = 0 set flip-flops F1 into working order, and resets B1 into the initial state. From output F1 of inverter N63 a logic 1 signal enables the operation of gate K65. At output $\overline{B1}$ of inverter N49 a logic 1 signal is generated, which through gate K94 analogous with the description of the Addition operation disables the operation of the MR register. As a result the first of the read and write cycles of the 16th byte do not produce the re-writing of the code of the sign of the number in the MR register.

At the end of the first read cycle a positive voltage drop from output LES of inverter N25 through gate K65 and the differentiating circuit with $\overline{MZ} = 0$ sets flip-flop ÜBER into the working order. A positive voltage drop of the ÜBER output of the flip-flop through the differentiating circuits with $\overline{R}$ = 0 set flip-flops E1 and E2 into the working order. Clock pulses S through gates K50 and K60 and the differentiating circuits with VER = 0 reset flip-flops E1 and E2 into the initial state.

The second read cycle produces re-writing of the "minus" sign code (0001) from the four ferrite core planes of the 16th byte of the AC0 register into the four flip-flops of register A. Flip-flop A1 is set into the working order. At the end of the read cycle a positive voltage drop of the LES output of inverter N25 through gates K28, K65 and K68 differentiation chains reset flip-flops A1, ÜBER and MZ into the initial state. A positive voltage drop of output A1F through the differentiating circuit with SUB = 0 sets flip-flop E1 into the working order.

Gate K98 is enabled state, and from the output of inverter N39 a logic 0 signal enters the collector input and disables the operation of flip-flop A2. Sequential clock pulses S through gate K50 and the differentiating circuit with VER = 0 resets flip-flop E1 into the initial state. From output E1 of inverter N13 a logic 0 signal enables gate K34. A positive voltage drop from the output of gate K34 does not change the initial state of the flip-flop A2.

As a result of the inversion of the sign of the operations result the second read and write cycle produces stores the code of the positive "plus" sign (0000) from the four flip-flops of register A into the four ferrite core planes of the 16th byte of the AC0 register. The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. Sequential pulse S1 through gates K142 and K194, the differentiating circuits with Z+E8=0 resets flip-flop R into the initial state and sets Z16 into the working order.

A positive voltage drop of the R output of inverter N58 through the differentiation circuits reset flip-flops F1 and E3 into the initial state. After setting flip-flop Z16 into the working order the Z counter starts, whose operation ensures the display of the subtrahend and sign of the number written into the four ferrite core planes of the MR register 000000000000071.

0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0111 0001

Completion of the Subtraction operation results in the difference sum of 44 and sign of the number being stored into the appropriate four bits of ferrite cores of the AC0 register.

0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0100 0100

III.3.9. Subtraction with MR < AC0.

Based upon Subtraction of the numbers in the example below let us examine the sequence of operation:

$$
\begin{array}{r}
\text{AC0} - 157 \\
\underline{\text{MR} - \ \ 23} \\
\text{AC} - 134
\end{array}
$$

The sequence of completing the operation is analogous to the description in the example of subtracting MR > AC0.

The Subtraction operation of the four flip-flops of register A occurs in the following order. During the first read and write cycle of the 1st byte of the MR register occurs the storage of the number 3 (0011) into the four flip-flops of register A and also the re-writing of the number 3 (0011) back into the four ferrite core planes of the MR register. During the second read and write cycle of the 1st byte of the AC0 register occurs the storage of the number 7 (0111) in the four flip-flops of register A and the completion of the Subtraction operation with the re-writing of the arithmetical addition of the byte into the four ferrite core planes of the AC0 register.

	Four flip-flops of the A register
1. First read and write cycle.	0011
2. Second read and write cycle	0111
3. Correction	1100
4. Arithmetical addition of the 1st byte	0110
	0110

5. The state of flip-flop ÜBER - working
Subtraction of the 2nd and next bytes are carried out in a sequence, analogous to the description of the 1st byte.

1. First read and write cycle.	0010
	0101
2. Second read and write cycle	1101

3. Subtraction of the unit of the transfer of the four bits of low-order digit   —   1
                                                                                         _ 1100
4. Correction   0110
5. Arithmetical addition of the 2nd byte   0110

6. The state of flip-flop ÜBER - is working
    subtraction of the 3rd byte:
1. First read and write cycle   _ 0000
                                                                                          0001
2. Second read and write cycle   _ 1111
3. Subtraction of the unit of the transfer   0001
                                                                                        _ 1110
4. Correction   0110
5. Arithmetical addition of the 3rd byte   1000
6. The state of flip-flop ÜBER - is working
    subtraction of the 4-15th bytes:
1. First read and write cycle   _ 0000
2. Second read and write cycle   0000
                                                                                          0000
3. Subtraction of the unit of the transfer   0001
                                                                                        _ 1111
                                                                                          0110
4. Correction   1001
5. Arithmetical is the addition of 4th byte
6. The state of flip-flop ÜBER - is working.

After subtraction of the 15th byte in register AC0 will be written the arithmetical addition and sign code of – 999999999999866

$$\begin{pmatrix} 0001 \ 1001 \ 1001 \ 1001 \ 1001 \ 1001 \ 1001 \ 1001 \ 1001 \ 1001 \ 1001 \ 1001 \ 1001 \ 1000 \ 0110 \ 0110 \\ S16 \hspace{10cm} S1 \end{pmatrix}$$

Flip-flop ÜBER is located in running order, and the Z counter switched for control of the 16th byte.

A positive voltage drop of output Z8 of inverter N84 through gate K140 and the differentiating circuit resets flip-flop B1 into the initial state. From output ÜBER of inverter N22 a logic 1 signal enters the control input of the differentiating circuit and blocks the setting of flip-flop F1 into the working order. From output F1 of inverter N63 a logic 0 signal disables the operation of gate K65 and the resetting of flip-flop MZ into the initial state.

The sign of the number is inverted during the read and write cycles of the 16th byte in the usual sequence and in the 16th byte of the AC0 register is written the code of positive "plus" sign (0000).

The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16} = 0$ resets flip-flop Z16 into the initial state.

5*

After resetting flip-flop Z16 into the initial state at output S16 of inverter N87 is formed a positive voltage drop, which through gate K183 and the differentiating circuit with F1 = 0 sets flip-flop Z1 into the working order which increments the Z counter. Simultaneously a positive voltage drop from the output of gate K183 through the differentiating circuit with $\overline{F3} = 0$ sets flip-flop F1 into the working order.

Flip-flop B1 is in the initial state, and from output $\overline{B1}$ of inverter N49 a logic 1 signal disables gate K94. From the output of the disabled gate a logic 1 signal is fed to the input of inverter N38. From output MRS of the inverter a logic 0 signal enters input U, it disables the operation of gate K6 for administration of the MR register. Flip-flop MZ is located in running order, and at output SUB of inverter N47 a logic 1 signal is generated, which completes the Subtraction operation.

During the Z counter cycle 000000000000000 occurs the subtraction of the complement 999999999999866 and the inversion of the code of the sign of the number of the AC0 register. As a result of completing the operation in register AC0 will be written the straight number – 000000000000134.

(0001 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0001 0011 0100)

After the inversion of the sign of the number in the AC0 register the disconnection of the Z counter, the resetting of the corresponding flip-flops into the initial state and display of the subtrahend occurs in a sequence, analogous to the description of the example of Subtraction with MR > AC0.

III.3.10.   Re-writing the information in AC0 → MR and the start of display.

Pressing the result key "=" after completion of an algebraic Addition accomplishes the operation of rewriting with erasure of the information from register AC0 in the MR register.

The closed contact of the key through the encoder diodes of the functional keyboard connects a logic 0 signal to the inputs of the keyboard filters L21 and L25. From outputs FU0 and (=)0 of the circuits logic 0 signals enter the controlling inputs of the differentiating circuits of the B4 and VOR flip-flops.

Pulse EING through the differentiating circuits with the signals FU0 = 0 and (=)0 = 0 set flip-flops B4 and VOR into the working order.

In the sequence of describing section III.2.3 occurs the preparation for the completion of the operation of rewriting. After the end of the preparatory part of the operation, pulse S1 through gate K186 sets flip-flop Z1 and increments the Z counter with EING=1. During incrementation of the Z counter is carried out the operation of rewriting AC0 → MR with the working order of flip-flop F2.

The setting of flip-flop F2 into the working order proceeds with the start of the operation of algebraic Addition from the "plus" or "minus" keys.

Operational control of the MR and AC0 registers occurs in the following order. Gate K118 is opened with U = 1 and LES = 1, at the AC0 output of inverter N45 a logic 1 signal is generated, which ensures operational control of the AC0 register. With U = 1 and SCHREIB = 1 gates K118 and K128 will be in the conducting state. At output AC0 of inverter N45 a logic 0 signal is generated, which disables the operation of the AC0 register. At output MRS of inverters N29 and N38 a logic 0 signal is generated only with AC0 = 1. Remaining time at output MRS a logic 1 signal is generated, which ensures operational control of the MR register. With the V = 1 gate K85 is enabled. From output HV of inverter N34 a logic 0 signal enters the input and disables the operation of the amplifiers of reproduction.

The first read cycle reads from the four ferrite core planes of the 1st byte of the AC0 register into the four flip-flops of register A.

The first write cycle rewrites the four flip-flops of register A into the four ferrite core planes of the 1st byte of the MR register. As a result rewriting occurs the distortion of the digital information of the byte of the MR register.

The second read cycle reads from the four ferrite core planes of the 1st byte without storing into the four flip-flops of register A and ensures the erasure of the information of the MR register.

The second write cycle rewrites information from the four flip-flops of register A into the four ferrite core planes of the 1st byte of the MR register. The rewriting of the remaining 14 bytes and sign of the number occurs analogously.

The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16} = 0$ resets flip-flop Z16 into the initial state. From output S16 of inverter N87 a positive voltage drop through gate K141 sets flip-flop R into the working order. A positive voltage drop from output $\overline{R}$ of inverter N57 through the differentiating circuit with $\overline{B4} = 0$ resets flip-flop F2 into the initial state. Sequential clock pulses S through gate K134 with $\overline{R} = 0$ resets flip-flop B4 into the initial state. The following pulse S1 through gate K142 with Z+E8 = 0 resets flip-flop R into the initial state. Simultaneously pulse S1 through gate K194 and the differentiating circuits sets flip-flop Z16 into working, and resets $\overline{VOR}$ into the initial state.

After rewriting AC0 → MR in the usual sequence occurs the display of the information, which has been written into the MR register.

Pressing a result "=" key with the initial state of flip-flop F2 ensures rewriting MR → MR in the sequence, analogous to the description of the rewriting AC0 → MR.

In this case gate K130 is enabled. From output AC0 of inverter N45 a logic 0 signal enters the input, enables gate K8 and disables the operation of the AC0 register. Consequently, the read cycles produce the rewriting of the information of the four bits of the MR register.

III.3.11. Re-writing the information in AC0 → MR and the start of display.

Pressing a key for an intermediate sum "▼I", "▼II", "▼III" after the completion of the operation of algebraic Addition accomplishes the operation of recalling without erasure the algebraic sum contents of one of the AC0 registers into register MR.

1. The contact of the "▼I" key through the encoder diodes of the functional keyboard connects a logic 0 signal to the inputs of the keyboard filters L25 and L18.

2. The contact of the "▼II" key connects a logic 0 signal to the inputs of the keyboard filters L25 and L19.

3. Analogously the contact of the "▼III" key connects a logic 0 signal to the inputs of the keyboard filters L25, L28, L19.

At the appropriate outputs FU0, (I), (II)0 of the keyboard filters logic 0 signals are generated, which enter the controlling inputs of the differentiating circuits of flip-flops VOR, F4 and F5.

By pressing the "▼I" key an EING pulse by a positive voltage drop through the differentiating circuits with FU0, (I)0 = 0 set flip-flops VOR and F4 into the working order and ensures operational control of register AC1. Analogously the operation of the "▼II" key ensures the setting of flip-flops VOR and F5 in working order and control of register AC2.

Pressing the "▼III" key ensures the setting of flip-flops VOR, F4 and F5 in working order and control of register AC3.

In the description in section III.2.3 occurs the preparation for the completion of the rewriting operation. After the end of the preparatory part of the operation a pulse S1 through gate K186 sets flip-flop Z1 incrementing the Z counter with EING2 = 1.

During the counting cycle the operation of rewriting without the erasure of $AC_N \rightarrow MR$ is carried out, gate K126 is in the disabled state. Gate K118 with U = 1 is enabled. From the output of gate K118 a logic 1 signal through gate D21 is fed to the input of inverter N43. From the output of the inverter a logic 0 signal through gate D23 is fed to the input of inverter N44. From output AC of the inverter a logic 1 signal enters the inputs of gates K9, K10 and K11, and ensures the control of one of the AC registers.

At output MRS of inverters N38 and N29 with V= 1 a logic 1 signal is generated, which ensures the operation of the MR register.

The first read cycle stores from the four ferrite core planes of the 1st byte of register AC_N into the four flip-flops of register A.

The first write cycle rewrites from the four flip-flops of register A into the four ferrite core planes of the 1st byte of register AC_N.

The second read cycle reads from the four ferrite core planes of the 1st byte of the MR register without storing into the four flip-flops of register A. (Gate K85 it is opened, at output HV it a logic 0 signal is generated, which disables the operation of the write amplifier). The second read cycle rewrites from the four flip-flops of register A into the four ferrite core planes of the 1st byte of the MR register.

The rewriting of the remaining 14 bytes and sign of the number occurs analogously.

The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state. A positive voltage drop of the S16 output of the inverter through gate K141 sets flip-flop R into the working order. Sequential pulse S1 through gate K142 with Z+E8 = 0 resets flip-flop R into the initial state. A positive voltage drop of output R of inverter N58 through the differentiating circuit resets flip-flop F4 (F5) into the initial state. Simultaneously pulse S1 through gate K194 and the differentiating circuits with Z+E8 = 0 sets flip-flop Z16 into the working order and resets VOR into the initial state.

After rewriting $AC_N \rightarrow MR$ in the usual sequence occurs the display of the information, written into the MR register. Pressing a corresponding key for a final sum "* I", "* II", "* III" performs the operation of recalling with erasure the algebraic sum contents of one of the registers AC_N into the MR register. The sequence of completing the operation corresponds to the description of recall without erasure. With the completion of the operation flip-flop F6 is located in running order. From output F6 of inverter N77 a logic 1 signal enables the operation of gate K125. During the completion of the first write cycle gate K125 is enabled. From the output of gate K125 a logic 1 signal through gate D23 is fed to the input of inverter N44. At output AC0 of the inverter a logic 0 signal is generated, which through gates K9, K10 and K11 disables the operation of the corresponding AC register.

Consequently, during each first write cycle from the four flip-flops of register A into the four ferrite core planes of register AC_N rewriting does not occur.

III.4.   Multiplication.

III.4.1. Entry of cofactors.

Based upon Multiplication of the numbers in the example below let us examine the sequence of operation:

$$(-135,00) \text{ x } (+25,00) = -3375,00.$$

The decimal point switch is set to position "2" (K = 2).

Introduction and the display of the first cofactor -135,00 occurs in a sequence, analogous to the description of sections III.2; III.2.1; III.2.4.

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
AC0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MR	1	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0

After loading the first cofactor by pressing the Multiplication "X" key locks the corresponding contact and through the functional keyboard encoder diodes connects a logic 0 signal to the inputs of the keyboard filters L20 and L25. From the outputs of diagrams (X)0, FU0 a logic 0 signal enters the control inputs of the differentiating circuits of flip-flops B2 and VOR. Pulse EING through the differentiating circuits set flip-flops VOR and B2 into the working order.

After setting the VOR flip-flop there occurs a sequence, analogous to the description in section III.2.3, for preparation of the completion of the operation of Multiplication. I.E. shift and installation of the first cofactor in the MR register in accordance with the assigned degree of accuracy and the Z counter cycle with EING2 = 1.

During the Z counter cycle the rewriting operation MR $\rightarrow$ MD/MR is performed with the erasure in register MD of the previously written information. During the rewriting control of the MR register occurs with U = 1. Control of the MD register is ensured by gate K101 with V=1.

During the first read and write cycles the rewriting of the number 0 (0000) in the 1st byte of the MR register occurs.

During the second read cycle storage from the four ferrite core planes of the 1st byte of the MD register into the four flip-flops of register A does not occur. Gate K85 with the V = 1 is enabled. From the output of gate K85 a logic 1 signal enters through gate D14 to the input of inverter N34. At output HV of the inverter a logic 0 signal is generated, which disables the operation of the write amplifiers (erasure of information).

During the second write cycle rewriting occurs from the four flip-flops of register A into the four bits of the 1st byte of the ferrite cores of the MD register.

Reading and writing in the 2nd byte of registers MR and MD occurs analogously with reading and writing in the 1st byte.

During the first read cycle storage occurs of the number 5 (0101) from the 3rd byte of the MR register into the four flip-flops of register A.

During the first write cycle the number 5 (0101) from the four flip-flops of register A is written into the 3rd byte of the MR register.

During the second read cycle from the four ferrite core planes of the 3rd byte of the MD register readout occurs without storage into the four flip-flops of register A, I.E. The erasure of the information 3rd byte of the MD register.

In the second write cycle from the four flip-flops of register A the rewriting of the number 5 (0101) into the four ferrite core planes if the 3rd byte of the MD register occurs.

The rewriting of the remaining digital bytes and sign of the number occurs analogously.

The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. A positive voltage drop on the S16 output of inverter N87 through gate K141 sets flip-flop R into the working order.

Sequential pulse S1 through gates K142 and K194 and the differentiating circuits with Z+E8 = 0 reset flip-flops VOR and R into the initial state and sets Z16 into the working order.

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MD	0	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0
AC0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MR	1	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0

From output $\overline{S16}$ of inverter N88 a logic 0 signal enters the control input of the differentiating circuit of the Z16 flip-flop. The VLS pulse of the 16th byte through the differentiating circuit resets flip-flop Z16 into the initial state and turns off the Z counter. Flip-flop B2 remains set.

After stopping the Z counter, pulse S1 through gate K186 sets flip-flop Z1 into the working order and enables the Z counter for display of the first cofactor. The entry of the second cofactor occurs in a sequence, analogous to the description of the entry of the first cofactor. After the entry of the second cofactor the result "=" key is pressed. The contact of the key operates and through the diodes of the functional keyboard encoder and connects a logic 0 signal to the inputs of the keyboard filters L21 and L25. From outputs (=)0 and FU0 a logic 0 signal enters the control inputs of the differentiating circuits of flip-flops VOR and B4.

A positive voltage drop of pulse EING through the differentiating circuits set flip-flops B4 and VOR into the working order. After setting of flip-flop VOR into the working order, a sequence, analogous to the description in section III.2.3, preparation for the completion of the Multiplication operation occurs, I.E. installation and shift of the second cofactor in the MR register in accordance with the assigned degree of accuracy and the Z counter cycle with EING2 = 1. During the Z counter cycle the initial state of flip-flop F2 ensures rewriting of the information MR → MR is analogous with the description in section III.3.10. (The working order of flip-flop F2 accomplishes the operation of rewriting information from AC0 → MR with the erasure of the information in the AC0 register.)

At the end of the MR → MR rewriting operation the VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16. A positive voltage drop at the S16 output of inverter N87 through gate K141 sets flip-flop R into working order. Sequential pulse S1 through gate K194 and the differentiating circuit with Z+E8 = 0 sets flip-flop Z16 and resets VOR into the initial state.

From output $\overline{VOR}$ of inverter N59 a logic 1 signal disables gate K136.

As a result of the enabled state of the gate at output $\overline{MUL}$ of inverter N52 a logic 0 signal is generated, and at the output MUL of inverter N53 - a logic 1 signal.

In accordance with the example, after the entry of the second cofactor the arrangement of the information written in the registers corresponds to the following table:

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MD	0	0	0	0	0	0	0	0	0	0	0	0	3	5	0	0
AC0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MR	1	0	0	0	0	0	0	0	0	0	0	0	2	5	0	0

III.4.2. Analysis of the signs of cofactors.

Analysis of the signs of cofactors is carried out after the preparatory part of the Multiplication operation. As a result of the analysis of signs the state of the MZ flip-flop determines the sign of work. The initial state of the flip-flop corresponds to the sign of work "plus", and the working state - to s "minus".

The working order of the Z16 flip-flop ensures control of the sign digit of cofactors.

Gate K102 with U = 1 is in the enabled state. At output MDS of inverter N42 a logic 1 signal is generated, which is fed to gate K7 and ensures operational control of the MD register. On the MRS output of inverters (N28)* N38 and (N39)* N29 with the V and LES = 1 a logic 1 signal is generated, which is fed to gate K6 and ensures control of the MR register. Gate K123 with the V and SCHREIB = 1 is in the enabled state. Consequently, at output AC0 of inverter N45 a logic 1 signal is generated, which is fed to gate K8 and ensures control of the AC0 register.

With the completion of the analysis of the cofactor signs there are four possible results.

1)   (-MD) x (-MR).

The first read cycle stores the "minus" sign code (0001) from the four ferrite core planes of the MD register into the four flip-flops of register A.

The first write cycle rewrites the "minus" sign code (0001) from the four flip-flops of register A into the four ferrite core planes of the MD register (MDS = 1.).

A positive voltage drop of the U output of inverter N27 through gate K132 and the differentiating circuit with F3 = 0 resets flip-flop A1 into the initial state.

A positive voltage drop of output A1 of inverter N5 through gate K157 sets flip-flop MZ into the working order.

* Note -
The N38 and N29 gate numbers listed here are corrections from the original Russian manual in which they were listed as N28 and N39, this did not match the circuit and logic drawings.

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Simultaneously a positive voltage drop of output A1F through the differentiating circuit with SUB = 0 sets flip-flop E1 into the working order. Sequential clock pulses S through gate K50 and the differentiating circuit with VER = 0 resets flip-flop E1 into the initial state. (Inversion of the flip-flop A2 through gate K34 it is disabled by the opened state of gate K98.)

The second read cycle stores the "minus" sign code from the four ferrite core planes of the MR register into the four flip-flops of register A (MRS = 1). Flip-flop A1 sets into the working order, and at output C1 of inverter N4 a logic 0 signal is generated. Gate K43 with V = 1 is in the enabled state, at outputs C4 and C8 of inverters N8 and N10 we obtain logic 0 signals.

The second write cycle writes the record of the X1 marker (in this case 1101) into the 16th byte of the AC0 register (AC0 = 1). The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. Simultaneously pulse VLS through gate K172 and the differentiating circuits resets flip-flop A1 into the initial state and sets F4 into the working order. A positive voltage drop from output A1 of inverter N5 through gate K157 resets flip-flop MZ into the initial state. Simultaneously a positive voltage drop from output A1F through the differentiating chain with SUB = 0 sets flip-flop E1 into the working order. Sequential clock pulses S through gate K50 reset flip-flop E1 into the initial state.

Thus, the initial state of flip-flop MZ determines the positive sign of work.

From output $\overline{F4}$ the inverter N72 a logic 0 signal disables the operation of gate K43. A positive voltage drop from the Z16 flip-flop output through the differentiating circuit when to $\overline{R}$ = 0 sets flip-flop F3 into the working order. Simultaneously from output S16 a logic 0 signal enables gate K196. A positive voltage drop from output S16 through gate K147 sets flip-flop F1 into the working order. From output $\overline{F3}$ a logic 0 signal enters the input and disables the operation of gates K157 and K98. From output F3 a logic 1 signal enters the control input of the differentiating circuit and disables the operation of gate K132.

After the analysis of the cofactor signs and storage of the X1 marker the arrangement of the written information in the registers corresponds to the following table:

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MD	0	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0
AC0	X1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MR	1	0	0	0	0	0	0	0	0	0	0	0	2	5	0	0

2)   (+MD) x (+MR).

The read and write cycles do not change the initial state of flip-flops A1 and MZ. During the second write cycle in the 16th byte is written the X1 marker (1100). The initial state of flip-flop MZ determines the positive sign of work.

3)   (+MD) x (-MR).

The first read and write cycles do not change the initial state of flip-flops A1 and MZ.

The second read and write cycles are carried out in a sequence, analogous to the description of the example (-MD) x (-MR), but in this case the MZ flip-flop sets into the working order. In the 16th byte of the AC0 register is written the X1 marker (1101). The working order of flip-flop MZ determines the negative sign of work.

4)   (-MD) x (+MR).

The first read and write cycles are carried out in a sequence, analogous to the description of the example (-MD) X (-MR), during the second read cycle flip-flop A1 does not change its reset state. Flip-flop MZ remains in running order.

During the second write cycle in the 16th byte the X1 marker (1100) is written.

The working order of flip-flop MZ determines the negative sign of work. After the completing the analysis of the cofactors signs, flip-flops B2 and R remain in running order.

III.4.3.   Interrogation and shift of the information in registers AC0 and MR

The cycle of interrogation further determines the operational regime of the arithmetic-logic unit depending on the information written into the 16th byte of the MR register, where in the 16th byte of the MR register is located:

A)   0000 - occurs the subtraction $0000 - 0001 = 1001$, after which is included the shift of information in registers AC0 and MR;

B) $0001 \div 1001$ - occurs subtraction 0001, after which the operation of adding $MD + AC0 \rightarrow AC0$ is carried out;

C)   X1 marker - the Multiplication operation is turned off directly.

After the analysis of the signs of an example sequential pulse S1 through gate K194 and the differentiating circuit with $Z+E8 = 0$ sets flip-flop Z16 into the working order and the Z counter is incremented. From output S16 of inverter N87 a logic 1 signal disables gate K116, as a result of which at outputs ADD1 and ADD of inverters N46 and N48 logic 0 signals are generated. At output SUB of inverter N47 a logic 1 signal is generated. A positive voltage drop from output ADD1 of inverter K46 through the differentiating circuit with $\overline{MUL} = 0$ sets flip-flop ÜBER into the working order. A positive voltage drop from output $\overline{UBER}$ through the differentiating circuits with $\overline{R} = 0$ set flip-flops E1 and E2 into the working order,

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so clock pulses S consecutively through gates K60 and K50 reset flip-flops E1 and E2 into the initial state. On the MRS output of inverters N38 and N29 with U = 1 and LES = 1, logic 1 signals, which ensure control of the operation of the MR register, are generated through gate K6.

The first read and write cycles of the 16th byte does not change the initial state of the four flip-flops of register A and the ferrite cores of the MR register. Gate K82 with U = 1 and SCHREIB = 1 is enabled. At output MR of inverters N29 and a logic 0 signal is generated, which through gate K6 disables the operation of the MR register.

The second read cycle of the 16th byte of the MR register does not change the initial state of the four flip-flops of register A. A positive voltage drop at the LES output of inverter N25 through gates K28 and K68 sets flip-flop A1 into the working order and resets ÜBER into the initial state. A positive voltage drop from output C1 of inverter N4 through the differentiating circuit with ADD = 0 sets flip-flop E1 into the working order. The following clock pulse S through gate K50 with VER = 0 resets flip-flop E1 into the initial state.

A positive voltage drop from output E1 of the flip-flop through gate K34 sets flip-flop A2 into the working order. A positive voltage drop from output C2 of inverter N6 through the differentiating circuit with ADD = 0 sets flip-flop E2 into the working order.

The following clock pulse S through gate K60 and the differentiating circuit when $\overline{E2}$ = 0 resets flip-flop E2 into the initial state. A positive voltage drop from output E2 of the flip-flop through gate K38 sets flip-flop A4 into the working order. A positive voltage drop from output C4 of inverter N8 through the differentiating circuit with ADD = 0 sets flip-flop E4 into the working order. Following clock pulse S through gate K60 and the differentiating circuit when $\overline{E4}$ = 0 resets flip-flop E4 into the initial state.

A positive voltage drop from output E4 of the flip-flop through gate K42 sets flip-flop A8 into the working order. A positive voltage drop from output C8 of inverter N10 through the differentiating chain with ADD = 0 sets flip-flop E8 into the working order. The following clock pulse S through gate K70 and the differentiating circuit with S1 = 0 resets flip-flop E8 into the initial state. A positive voltage drop from output E8 of inverter N21 through gate K64 and the differentiating circuit with U = 0 sets flip-flop ÜBER into the working order. A positive voltage drop from output $\overline{UBER}$ of the flip-flop through the differentiating circuits with $\overline{R}$ = 0 set flip-flops E1 and E2 into the working order.

Following clock pulse S through gate K60 and the differentiating circuit when $\overline{E2}$ = 0 resets flip-flop E2 into the initial state. A positive voltage drop from output E2 of the flip-flop through gate K38 resets flip-flop A4 into the initial state.

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Sequential clock pulses S through gate K50 and the differentiating circuit with VER = 0 resets flip-flop E1 into the initial state.

A positive voltage drop from output E1 of the flip-flop through gate K34 resets flip-flop A2 into the initial state. As a result of the transfer of the overflow bits a subtraction is executed 0 - 1 (0000 - 0001). In the four flip-flops of register A is written number 9 (1001).

The second write cycle rewrites the number 9 (1001) from the four flip-flops of register A into the four ferrite core planes of the 16th byte of the MR register.

The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. A positive voltage drop from output Z16 of inverter N87 through gate K148 and the differentiating circuit with ADD = 0 resets flip-flop F1 into the initial state.

After interrogation of the arrangement of the information, the contents written into registers MD, AC0, MR, correspond to the following table:

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MD	1	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0
AC0	X_1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MR	9	0	0	0	0	0	0	0	0	0	0	0	2	5	0	0

Sequential pulse S1 through gate K155 and the differentiating circuits with $\overline{UBER}$= 0 set flip-flops Z1 and VER into the working order incrementing the Z counter. The setting of flip-flop VER into the working order accomplishes the shift of the information in registers AC0 and MR. At output $\overline{VER}$ of inverter N67 a logic 0 signal, enters the collector input, sets and blocks in running order flip-flop UV. Gates K124 and K123 with the V, LES and SCHREIB = 1 alternately be in the conducting state. As a result with the V = 1 from the output of gate D21 a logic 1 signal is fed to the input of inverter N43. From the output of the inverter a logic 0 signal is fed to the input of gate D22. From the output of the gate a logic 0 signal is fed to the input of inverter N45. At output AC0 of the inverter we obtain a logic 1 signal, which through gate K8 ensures control of the AC0 register. Shift of the information in register AC0 is carried out in a sequence, analogous to the description of shift with the introduction.

During the Z counter cycle shifting of the number 0 (0000) occurs from the 1st through to the 15th byte.

The read cycle stores the X1 marker (1100) of the 16th byte of the AC0 register into the four flip-flops of register A.

The write cycle rewrites the number 0 (0000) from four flip-flops of register E into the four ferrite core planes of the 16th byte of the AC0 register.

The VLS pulse of the 16th byte through the differentiating circuit reset flip-flops A4 and A8 of register A into the initial state. Positive voltage drops at the A4 and A8 outputs of inverters N9 and N11 through the differentiating chains with SUB = 0 set flip-flops E4 and E8 into the working order. Simultaneously a VLS pulse through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state.

A positive voltage drop from VLS output of inverter N87 through gate K182 and the differentiating chain with F6 = 0 sets flip-flop Z1 into the working order. Simultaneously a positive voltage drop from output S16 through gate K147 and the differentiating chain with F1 = 0 sets flip-flop F1 into the working order, from output $\overline{F1}$ of inverter N62 a logic 0 signal enters the inputs and shut gates K123 and K124.

As a result at output AC0 of inverter N45 a logic 0 signal is generated, and at the output MRS of inverters N29 and N38 - a logic 1 signal, which through gate K6 ensures operational control of the MR register.

The read cycle stores the number 0 (0000) from the four ferrite core planes of the 1st byte into the four flip-flops of register A.

The write cycle rewrites the X1 marker (1100) from the four flip-flops of register E into the four ferrite core planes of the 1st byte of the MR register.

The VLS pulse of the 1st byte through gate K187 increments the Z counter, which ensures control of the 2nd byte.

The shift of the information of the 2-15th bytes of the MR register is carried out in a sequence, analogous to the description of shift with the introduction.

The read cycle stores the number 9 (1001) from the four ferrite core planes of the 16th byte of the MR register into the four flip-flops of register A.

A write cycle in accordance with the example rewrites the number 0 (0000) from the four flip-flops of register E into the four ferrite core planes of the 16th byte of the MR register. The VLS pulse of the 16th byte through the differentiating chains reset flip-flops A1 and A8 into the initial state and stores the number 9 (1001) from the four flip-flops of register A into the four flip-flops of register E. Simultaneously a VLS pulse through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. A positive voltage drop from output S16 of inverter N87 through gate K148 and the differentiating circuit with $\overline{F1}$ = 0 resets flip-flop VER into the initial state. A positive voltage drop from output VER of inverter N68 through the differentiating chains reset flip-flops UV and ÜBER into the initial state. Sequential clock pulses S through gate K50 and the differentiating circuit with VER = 0 resets flip-flop E1 into the initial state. The following clock pulse S through gate K70 and the differentiating chain with S1 = 0 resets flip-flop E8 into the initial state.

After the shift of the information, the contents written into registers MD, AC0 and MR, correspond to the following table.

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MD	1	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0
AC0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MR	0	0	0	0	0	0	0	0	0	0	0	2	5	0	0	X_1

Sequential pulse S1 through gate K194 with Z+E8 = 0 sets flip-flop Z16 into the working order incrementing the Z counter to interrogate the 16th byte of the MR register.

Interrogation, subtraction 0-1 and shift of the information in registers AC0 and MR is carried out in a sequence, analogous to the description in section III.4.3. In accordance with the example of the last table after 11 cycles of interrogation and shifting, the number 2 (0011) is written into the 16th byte of the MR register.

As a result of the execution of 11 cycles of interrogation and shifting the information, the contents written into registers MD, AC0 and MR, correspond to the following table:

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MD	1	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0
AC0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MR	2	5	0	0	X_1	0	0	0	0	0	0	0	0	0	0	0

III.4.4. Interrogation and addition of the contents of registers
MD + AC0 → AC0.

 After the shift and writing of the number 2 (0010) into the 16th byte of the MR register the interrogation of the MR register is included in the usual sequence.

The first read cycle stores the number 2 (0010) from the four ferrite core planes of the 16th byte of the MR register into the four flip-flops of register A.

During the first write cycle gate K82 is enabled. From output MRS of inverters N29 and N38 a logic 0 signal enters gate K6 and disables the operation of the MR register. As a result rewriting of the number 2 (0010) into the 16th byte of the MR register does not occur.

The second read cycle stores the number 0 (0000) from the 16th byte of the MR register into the four flip-flops of register A.

A positive voltage drop from the LES output of inverter N25 through gate K68 and the differentiating chain with U = 0 resets flip-flop ÜBER into the initial state. Simultaneously a positive voltage drop of signal LES through gate K28 sets flip-flop A1 into the working order. A positive voltage drop from output C1 of inverter N4 through the differentiating circuit with ADD = 0 sets flip-flop E1 into the working order. Sequential clock pulses S through gate K50 and the differentiating circuit with VER = 0 resets flip-flop E1 into the initial state. A positive voltage drop from output E1 of inverter K13 through gate K34 resets flip-flop A2 into the initial state. As a result of the subtraction of 0010 – 0001 the transfer of the overflow bits occurred.

The second write cycle rewrites the number 1 (0001) from the four flip-flops of register A into the four ferrite core planes of the 16th byte of the MR register.

The VLS pulse of the 16th byte through the differentiating circuits with $\overline{S16} = 0$ reset flip-flops A1 and Z16 into the initial state and turns off the Z counter

A positive voltage drop from output S16 of inverter N87 through gate K148 and the differentiating circuit with ADD = 0 resets flip-flop F1 initial state. Sequential pulses S1 through gate K155 sets into the working order flip-flop Z1 and increments the Z counter.

During the operation of the Z counter an Addition operation is carried out for $MD + AC0 \rightarrow AC0$. Gate K103 with U = 1 is enabled. At output MDS of inverter N42 a logic 1 signal is generated, which enters gate K7 and ensures operational control of the MD register.

Gates K123 and K124 with V, LES and SCHREIB = 1 are alternately enabled. Consequently, with V = 1 from the AC0 output a logic 1 signal enters gate K8 and ensures operational control of the AC0 register. Completion of the addition operation $MD + AC0 \rightarrow AC0$ occurs in a sequence, analogous to the description of the operation of adding $MR + AC0 \rightarrow AC0$. The Add operation does not occur in the 16th byte. Gate K103 with U and $\overline{S16} = 0$ is disabled, so from output MDS of inverter N42 a logic 0 signal enters gate K7 and disables the operation of the MD register, as a result the cofactor sign remains in the MD register.

Pulse VLS through the differentiating circuit with $\overline{S16} = 0$ resets flip-flop Z16 into the initial state and turns off the Z counter.

A positive voltage drop from output S16 of inverter N87 through gate K147 sets flip-flop F1 into the working order.

After the first addition $MD + AC0 \rightarrow AC0$ the arrangement of the information, written into registers MD, AC0, MR, corresponds to the following table:

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MD	1	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0
AC0	0	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0
MR	1	5	0	0	X_1	0	0	0	0	0	0	0	0	0	0	0

Sequential pulse S1 through gate K194 and the differentiating circuit with Z+E8 = 0 sets flip-flop Z16 into the working order incrementing the Z counter for the interrogation of the 16th byte of the MR register.

During the interrogation occurs the subtraction of one from the four bits of the 16th byte of the MR register (0001 - 0001 = 0000), after Subtraction the Add operation of MD + AC0 → AC0 is implemented.

As a result the second addition of MD + AC0 → AC0 the arrangement of the information, written into registers MD, AC0, MR, corresponds to the following table:

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MD	1	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0
AC0	0	0	0	0	0	0	0	0	0	0	0	2	7	0	0	0
MR	0	5	0	0	X_1	0	0	0	0	0	0	0	0	0	0	0

During the following interrogation the subtraction of 1 from the four bits of the 16th byte of the MR register (0000 - 0001 = 1001) occurs. After the subtraction 0 - 1 the shift of the information of registers AC0 and MR is included.

As a result of the shift the arrangement of the information, written into registers MD, AC0, MR, corresponds to the following table:

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MD	1	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0
AC0	0	0	0	0	0	0	0	0	0	0	2	7	0	0	0	0
MR	5	0	0	X_1	0	0	0	0	0	0	0	0	0	0	0	0

The completion of the interrogation operation and adding MD + AC0 → AC0, interrogation and the shift of the information of registers AC0 and MR occurs to record the X1 marker (1100) into the 16th byte of the MR register.

In accordance with the example after five operations of interrogation and addition the arrangement of the information, written into registers MD, AC0, MR, correspond to the following table:

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MD	1	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0
AC0	0	0	0	0	0	0	0	0	0	0	3	3	7	5	0	0
MR	0	0	0	X_1	0	0	0	0	0	0	0	0	0	0	0	0

As a result of the completion of the 3-x operations of interrogation and shift of the information in registers AC0 and MR, the X1 marker (1100) will be written into the 16th byte of the MR register. The arrangement of the information, written into registers MD, AC0, MR, will correspond to the following table:

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MD	1	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0
AC0	0	0	0	0	0	0	0	3	3	7	5	0	0	0	0	0
MR	X_1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

III .4.5. Rejection of bytes and rounding.

After the record of the X1 marker (1100) into the 16th byte of the MR register, interrogation in the usual sequence is included. The first read cycle stores the X1 marker (1100) from the four ferrite core planes of the 16th byte of the MR register into the four flip-flops of register A. The flip-flops A4 and A8 invert into the working order. From outputs A4 and A8 of inverters N9 and N11 logic 1 signals enter the inputs and disables gate K56. At output X of inverter N18 a logic 1 signal, disables gate K73. A positive voltage drop from output LES of inverter K25 through gate K73 and the differentiating chains with ADD = 0 resets flip-flop F4 into the initial state and sets F5 into the working order. From output F5 of inverter N75 a logic 1 signal disables gate K52. A positive voltage drop from output G1 of inverter N12 through the differentiating circuit resets flip-flop A8 into the initial state.

The decimal point switch is set to position 2 (K = 2).

At outputs G220 and G110 of the switch filters logic 0 signals are produced, which enter the appropriate controlling inputs of the differentiating circuits of flip-flops Z1 and Z2. A positive voltage drop from output G1 of inverter N12 through the differentiating circuits with G220 and G110 = 0 set flip-flops Z1 and Z2 into the working order. The working order of flip-flops Z1 and Z2 creates control of the 3rd byte. A positive voltage drop from output S16 of inverter N87 through gate K148 and the differentiating circuit with ADD = 0 resets flip-flop F1 into the initial state. Simultaneously from output S16 a logic 0 signal enables gate K116.

As a result at outputs ADD1 and ADD of inverters N46 and N48 the signal levels change from 0 to 1.

During the first write cycle gates K82 and K95 are enabled. From output MRS of inverters N29 and N38 a logic 0 signal enters gate K6 and disables the operation of the MR register. Simultaneously on outputs AC, AC0 and MDS of inverters N44, N45 and N42 logic 0 signals are generated, which are fed to the input of gates K7 - K10 and block the operation of registers AC0, AC1, AC2, AC3 and MD. Consequently, the rewriting of the remainder of the X1 marker (0100) does not occur.

Gate K124 with V and LES = 1 is enabled. From output AC0 of inverter N45 a logic 1 signal enters gate K8 and ensures operational control of the AC0 register.

In accordance with the example during the second read cycle, from the four ferrite core planes of the 3rd byte of the AC0 register the number 0 (0000) is stored into the four flip-flops of register A. At output LES of inverter N25 is formed a positive voltage drop, which through gates K28 and K68 reset flip-flops ÜBER into the initial state and A1 into the working order.

The working order of flip-flops A1 and A4 correspond to storing in the flip-flops of the rounding off number 5 (0101). Flip-flop UV is in running order, from output V of inverter N28 a logic 1 signal disables gate K43. At outputs C1, C4 and C8 logic 0 signals are generated, which disable gates K24, K2 and K25, disabling the operation of the inhibit stages. Consequently, during the second write cycle the marker X2 (1101) is written in the four ferrite core planes of the 3rd byte of the AC0 register.

Pulse VLS of the 3rd byte through gate K187 increments the Z counter for control of the 4th byte. Simultaneously pulse VLS through gate K172 and the differentiating circuit sets flip-flop F4 into the working order. During the first of the read and write cycles for the 4th byte with U = 1 at outputs AC0, AC, MDS and MRS of inverters N29, N38, N42, N44 and N45 logic 0 signals are generated, which are fed to the inputs of gates K6, K7, K8, K9, K10 and K11 blocking the operation of registers AC0, MD, MR, AC1, AC2 and AC3. (Operational control of the MR register is blocked through gate K95).

After the first read and write cycles gate K124 with V = 1, LES = 1 and gate K123 with the V = 1, SCHREIB = 1 be enabled state. At output AC0 of inverter N45 a logic 1 signal, ensures control of the AC0 register.

The second read cycle stores the number 0 (0000) from the four ferrite core planes of the 4th byte into the four flip-flops of register A.

The second write cycle rewrites the number 0 (0000) from the four flip-flops of register A into the four ferrite core planes of the 4th byte of the AC0 register.

The VLS pulse of the 4th byte through gate K187 increments the Z counter for control of the 5th byte.

Re-writing of the remaining bytes of the AC0 register occurs in the analogous sequence.

The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16} = 0$ resets flip-flop Z16 into the initial state and turns off the Z counter. A positive voltage drop from output S16 of inverter N87 through gate K147 sets flip-flop F1 into the working order.

After recording the marker X2 the arrangement of the information, written into registers MD, AC0, MR, correspond to the following table:

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
D	1	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0
C0	0	0	0	0	0	0	0	3	3	7	5	0	0	X_1	0	0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

III.4.6. General case of rounding.

Prior to the beginning of the formation an X2 marker in the appropriate byte of the AC0 register is written one of the numbers from 0001 to 1001. During the second read cycle of four ferrite cores this number is rewritten into the four flip-flops of register A, where addition with the remainder of the X1 marker (0100) occurs.

A positive voltage drop of the output LES of inverter N25 through gate K68 resets flip-flop ÜBER into the initial state. Simultaneously a positive voltage drop LES through gate K28 changes the position of the A1 flip-flop. The setting of the flip-flop increases the number, written in the flip-flops of register A by one.

In the cases of storing a number of more than 4 (0100) into the four flip-flops of register A during the second read cycle of an operation in the usual sequence occurs the transfer of the overflow bits. As a result of the transfer a positive voltage drop from output E8 of the inverter N21 through gate K64 and the differentiating circuit with U = 0 sets flip-flop ÜBER into working order. During the second write cycle the formation and writing occurs of the X2 marker into the four ferrite core planes of this byte of the AC0 register. The X2 marker depending on the result of adding the counted number with rounding off number 5 (0101) can take values from 1100 to 1111.

The VLS pulse of this byte ensures the setting of flip-flop F4 into the working order and switching the Z counter for control of the next decade.

In the next decade the first read and write cycles are carried out without control of registers, I.E. At outputs AC0, AC, MDS and MRS of the corresponding inverters are manufactured logic 0 signals, which disables the operation of registers.

The second read cycle stores the information of the four ferrite core planes into the four flip-flops of register A. A positive voltage drop from output LES of inverter N25 resets flip-flop ÜBER into the initial state.

Simultaneously a positive voltage drop from output LES through gate K28 changes the position of the flip-flop A1 and ensures the addition of the number, counted from the byte of the AC0 register with the unit of rounding.

The second write cycle rewrites the result of the addition from the four flip-flops of register A into the four ferrite core planes of this byte of the AC0 register.

When as a result rounding is obtained the unit of transfer from the 16th byte of the AC0 register, the pulse VLS through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. Simultaneously pulse VLS through gate K182 sets flip-flop Z1 incrementing the Z counter. Flip-flop ÜBER remains in running order.

A positive voltage drop from output S16 of inverter N87 through gate K147 and the differentiating circuit with F1 = 0 sets flip-flop F1 into the working order.

From output $\overline{F1}$ of inverter N62 a logic 0 signal enables gate K95. As a result at output MRS of inverters N29 and N38 a logic 1 signal is manufactured, which ensures control of the MR register.

The first read cycle stores the number from the 1st byte of the MR register into the four flip-flops of register A.

During the first write cycle gate K82 enabled. At output MRS of the inverter a logic 0 signal is generated entering the input of gate K6 and blocking the operation of the MR register.

At the end of the second read cycle of the 1st byte of the MR register a positive voltage drop of the LES output of inverter N25 through gate K68 and the differentiating circuit with U = 0 resets flip-flop ÜBER into the initial state.

Simultaneously a positive voltage drop from output LES through gate K28 changes the state of the A1 flip-flop. As a result of this in the register A flip-flops the addition of the counted number and unit of transfer occurs.

During the second write cycle the result of the addition is rewritten from the four flip-flops of register A into the four ferrite core planes of the 1st byte of the MR register.

The Z counter cycle and the rewriting of the four ferrite core planes of the MR register occurs to the 16th byte inclusively. Flip-flop F1 remains set after stopping the Z counter.

III.4.7. Interrogation and shift of data from register AC0 to register MR.

After rounding and writing of the X2 marker interrogation is included and the shift of the information of registers AC0 and MR with recording of the X2 marker into the 16th byte of the AC0 register is carried out. As a result of the execution of 12 cycles of interrogation and shift the arrangement of information in registers MD, AC0 and MR correspond to the following table:

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MD	1	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0
AC0	0	X_2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MR	0	0	0	0	0	0	0	0	0	0	0	3	3	7	5	0

In the usual sequence the 13th interrogation is included and carries out the shift of the information in registers AC0 and MR.

The read cycle stores the last figure of work according to example 0 (0000) from the four ferrite core planes of the 16th byte of the AC0 register into the four flip-flops of register A.

In the flip-flops of register E is written the marker X2 (1101), that previously counted from the 15th byte of the AC0 register, the flip-flops E4 and E8 are located in running order. From outputs E4 and E8 the signals E enter the inputs and disable gate K59.

From output X of inverter N8 logic 1 signal disables gate K175.

The write cycle rewrites the X2 marker (1101) from the four flip-flops of register E into the four bits of ferrite cores of the 16th byte of the AC0 register.

The VLS pulse of the 16th byte through the differentiating circuits resets the four flip-flops of the A register into the initial state and stores the last figure of work 0 (0000) into the four flip-flops of register E.

Simultaneously a pulse VLS through gates K182 and K175 and the differentiating circuits with $\overline{S16}$ = 0, F6 =0, $\overline{MUL}$= 0 reset flip-flop Z16 into the initial state with Z1 and F6 into the working order.

A positive voltage drop from output S16 of inverter N87 through gate K147 and differentiating chain with F1 = 0 sets flip-flop F1 into the working order and ensures control of the MR register. The position of the Z counter ensures control of the 1st byte.

The read cycle stores the next-to-last number from the four ferrite core planes of the 1st byte of the MR register into the four flip-flops of the A register.

The write cycle rewrites the last figure of 0 (0000) from the four flip-flops of the E register into the four ferrite core planes of the 1st byte of the MR register, the sequential rewriting of information in the MR register ensures shift and record of work in accordance with the assigned degree of accuracy.

Flip-flop MZ is located it in running order and determines the negative sign of work. Pulse VLS through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state. A positive voltage drop from output S16 of the inverters through gates K147 and K148, the differentiating circuits with $\overline{F1}$ = 0 and $\overline{F6}$ = 0 reset flip-flops F1 and VER into initial state, a positive voltage drop from output VER of inverter N68 through a differentiating chain resets flip-flop ÜBER (transfer) into the initial state.

After the disconnection of the shift of work the arrangement of the information, written into registers MD, AC0, MR, correspond to the following table:

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MD	1	0	0	0	0	0	0	0	0	0	0	1	3	5	0	0
AC0	X_2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MR	0	0	0	0	0	0	0	0	0	0	0	3	3	5	0	0

III.4.8. Erasure of the AC0 register.

A sequential pulse S1 through gates K155 and K194, the differentiating circuits with Z+E8 = 0 set flip-flops Z1 and Z16 into the working order and increments the Z counter. Operation of the MR register is blocked by the enabled state of gate K95 with F3 = 1.

During the indexing of the Z counter at output AC0 of inverter N45 a logic 1 signal is generated, which ensures operational control of the AC0 register through gate K124 with the V = 1 and LES = 1, I.E. To the period of the second read cycle. With V = 1 and SCHREIB = 1 gate K123 is disabled with logic 0 signal at the input $\overline{F6}$. As a result at output AC0 of inverter N45 a logic 0 signal is generated, which enters gate K8 and disables the operation of the AC0 register, therefore, during the read cycle, the only storing of the contents of each byte of the four ferrite core planes into the flip-flops of register A occurs. The absence of rewriting from the four flip-flops of register A into the four ferrite core planes ensures the erasure of the information in the AC0 register.

The read cycle stores the X2 marker (1101) from the four ferrite core planes of the 16th byte into the four flip-flops of register A. Flip-flops A4 and A8 invert into the working order. From outputs A1, A4 and A8 of inverters N9, N11 logic 1 signals disable gate K56, at output $\overline{X}$ of inverter N17 is formed a positive voltage drop, which through gate K71 sets flip-flop E8 into the working order. From the (output)* input $\overline{E8}$ of inverter N21 a logic 0 signal enables gate K49. From output E of inverter N14 a logic 1 signal disables gate K166. From output M of inverter N69 a logic 0 signal enters gate K162 and blocks the shaping of the t and $\overline{t}$ pulses for the write cycle.

Sequential clock pulses S through gate K71 and the differentiating chain reset flip-flop S1 into the initial state. Pulse S1 through gate K74 and the differentiating chain sets flip-flop LES - SCHREIB into the working order.

* Note -

The $\overline{E8}$ signal is derived from the input of inverter N21, not the output as written in the original Russian manual, this did not match the original drawings.

Sequential clock pulses S through gate K70 and the differentiating circuit with S1 = 0 resets flip-flop E8 into the initial state. A positive voltage drop from output E8 of inverter N21 through gate K64 and the differentiating circuit with Ü = 0 sets flip-flop ÜBER into the working order. A positive voltage drop from the ÜBER output of the flip-flop through the differentiating circuits with $\overline{R} = 0$ set flip-flops E1 and E2 into the working order. Sequential clock pulses S through gate K60 and the differentiating circuit with $\overline{E2}$ = 0 resets flip-flop E2 into the initial state. A positive voltage drop of the E2 output of the flip-flop through gate K38 resets flip-flop A4 into the initial state.

A positive voltage drop from output A4F through the differentiating circuit with SUB = 0 sets flip-flop E4 into the working order. Sequential clock pulses S through gates K50 and K60 reset flip-flops E1 and E4 into the initial state. A positive voltage drop from output E1 of inverter N13 through gate K34 sets flip-flop A2 into the working order. A positive voltage drop from output E4F of the flip-flop through gate K42 resets flip-flop A8 into the initial state. A positive voltage drop from output A8 of inverter N11 through the differentiating circuit with SUB = 0 sets flip-flop E8 into the working order. The following clock pulse S through gate K70 resets flip-flop E8 into the initial state. From output $\overline{E8}$ of the flip-flop a logic 1 signal disables gate K49. From output E of inverter N14 a logic 0 signal enables gate K166. At output M of inverter N69 a logic 1 signal is generated, which accomplishes a write cycle. During the completion of the write cycle register AC0 is not governed.

The VLS pulse of the 16th byte in the differentiating chain reset flip-flops A1, A2 into the initial state and stores the number 3 (0011) into the four flip-flops of register E. The following clock pulses S through gates K50 and K60 reset flip-flops E1 and E2 into the initial state. Simultaneously pulse VLS through gate K182 and the differentiating circuits with $\overline{S16}$ =0 and F6=0 reset flip-flops B2 and Z16 into the initial state and turns off the Z counter. A positive voltage drop from output S16 of inverter N87 through gate K147 sets flip-flop F1 into the working order. From output B2 of the flip-flop a logic 0 signal enables gate K136. As a result at the MUL output of inverter N53 a logic 0 signal is generated, and at the output $\overline{MUL}$ of inverter N52 a logic 1 signal. Sequential clock pulses S through gates K66 and K134, the differentiating circuits with MUL = 0 and $\overline{R}$ = 0 reset flip-flops B4 and ÜBER into the initial state. Sequential pulse S1 through gates K142 and K194, and the differentiating circuits with Z+E8 = 0 reset flip-flops R into the initial and sets Z16 into the working order. A positive voltage drop from output R of inverter N58 through the differentiating circuits reset flip-flops F1, F3, F4, F5 and F6 into the initial state.

From output $\overline{R}$ of inverter N57 the signal disables gate K152. From output C1 of inverter N4 a logic 0 signal disables the operation of gate K24 for the inhibit driver BL1.

The working order of flip-flop Z16 determines control of the 16th byte. At output MRS of inverters N29 and N38 a logic 1 signal is generated, which ensures operational control of the MR register.

During the first read cycle the number 0 (0000) is stored from the ferrite cores of the 16th byte of the MR register into the four flip-flops of register A.

During the first write cycle gate K152 is enabled, at output C1 of inverter N4 a logic 0 signal is generated, which ensures the storage of the "minus" sign code 1 (0001) into the four ferrite core planes of the 16th byte of register MR.

During the second read cycle the "minus" sign code 1 (0001) is not stored from the 16th byte four ferrite cores of the MR register into the four flip-flops of register A. Gate K85 with V= 1 is enabled. From output HV of inverter N34 a logic 0 signal disables the operation of the read amplifiers.

During the second write cycle the "minus" sign code (0001) is rewritten into the 16th byte four ferrite cores of the MR register as a result of the enabled state of gate K152. Simultaneously a VLS pulse through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. Sequential pulse S1 through gate K186 and the differentiating circuit with X = 0 sets flip-flop Z1 into the working order and starts the Z counter for the display of work.

III.4, 9.   Register length overflow during Multiplication.

When work exceeds the permissible register length, I.E. it has more than 15 bytes, during the completion of the shift operation AC0 → MR occurs an overflow.

The VLS pulse of the 15th byte stores the previously counted number of the 15th byte of the MR register from the four flip-flops of register A into the four flip-flops of register E.

At one of the four flip-flops of register E outputs $\overline{E1}$, $\overline{E2}$, $\overline{E4}$ and $\overline{E8}$ a logic 0 signal is generated, which enables gate K49. From output E of inverter N14 a logic 1 signal enables gate K164. Simultaneously pulse VLS through gate K187 increments the Z counter for operational control of the 16th byte of the MR register.

At output S16 of inverter N87 a logic 1 signal is generated, which disables gate K164. From the output of gate K164 a logic 1 signal enters through gate D25 to the input of inverter N69.

From output M of inverter (N68)* N69 a logic 0 signal enters the input and disables gates K74 and K162.

Note *
The original Russian manual lists output M of inverter N68, this was incorrect and has been corrected to N69.

After disabling inputs the Z16 flip-flop remains in running order and ensures control of the 16th byte.

Consequently, gates K197 - K211 of the display anode amplifiers are in the non-conducting state. At the gate outputs logic 0 signals are generated, which disables the operation of the anode amplifiers and digital lamps.

By pressing the Lö key analogous with the description in section III.1 the erasure of the contents of the operational register occurs and so enables the display.

III.4.10. Exponentiation.

The Exponentiation operation or raising a number to the Nth degree is carried out in a sequence, analogous to a Multiplication operation.

As a result of entry of the first cofactor and entry of a Multiplication key a number will be written in registers MD and MR, raised to the degree, I.E. The first cofactor.

In contrast to a Multiplication operation, instead of the second cofactor should be entered the Exponentiation key "X^n".

The contact of the "X^n" key through the diodes of the functional keyboard encoder connects a logic 0 signal to the inputs of the keyboard filters L20, L21 and L25.

From outputs FU0, (X)0 (=)0 of the keyboard filters logic 0 signals enter the controlling inputs of the differentiating circuits of flip-flops B2, B4 and VOR.

A positive voltage drop of pulse EING through the differentiating circuits with (=)0, FU0, (X)0 = 0 set flip-flops B2, B4 and VOR into the working order.

After the setting of flip-flop VOR into the working order, a sequence, analogous to the description in section III.2.3, preparation for completing the exponentiation operation of the number into the Nth degree occurs, I.E. shift and installation of the second cofactor in the MR register in accordance with the assigned degree of accuracy and the Z counter cycle with EING2 = 1.

During the Z counter cycle flip-flop F2 is in the initial state and ensures in accordance with the description in section III.3.10 completion of the operation of rewriting the register MR → MR. As a result the Z counter cycle in the sequence, and analogous to the description of a Multiplication operation, at output MUL of inverter N53 a logic 1 signal is generated, which determines the completion of the usual Multiplication operation.

After the completion of the Multiplication operation the MR register will contain the number, elevated to the second degree. In the MD register remains the number, raised to the degree. Each following start of key "X^n" ensures completion of the Multiplication operation by a constant cofactor, I.E. The exponent of the raised number increases by one.

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III.5.   Division.

III.5.1. Dividend entry.

Based upon Division of the numbers in the example below let us examine the sequence of operation of:

$$12,07 \div 12,00 = 1,01$$

The decimal point switch is set to position 2 (K = 2). Entry and display of the dividend 12,07 occurs in a sequence, analogous to the description in section III.2.

After entering the dividend the Division key is pressed and the corresponding keyboard contact, connects a logic 0 signal to the inputs of keyboard filters L16 and L25, through to the diodes of the functional keyboard encoder. From the outputs of the keyboard filters (:)0 and, FU0 logic 0 signals enter the control inputs of the differentiating circuits of flip-flops B3 and VOR.

A positive voltage drop of the EING pulse through the differentiating circuits set flip-flops VOR and B3 into the working order.

As a result of setting of flip-flop VOR into the working order, the sequence analogous to the description in section III.2.3, occurs preparation for completion of the Division operation.

During the Z counter cycle with EING = 1 the rewriting of MR → MD/MR with erasure of the previous data in the MD register is carried out.

With completion of the rewriting operation, operational control of the following registers occurs:
MR with U= 1,
MD with the V = 1 through gate K101.

During the first read cycle the number 7 (0111) is stored from the four ferrite core planes of the 1st byte of register MR into the four flip-flops of register A.

In the first write cycle the number 7 (0111) is rewritten into the four ferrite core planes of the 1st byte of the MR register from the four flip-flops of register A.

During the second read cycle, the information from the four ferrite core planes of the 1st byte of the MD register is not stored into the four flip-flops of the A register. Gate K85 with V = 1 is disabled, and from the HV output of inverter N34 a logic 0 signal blocks operation of the write amplifiers. Consequently, with V= 1 and LES = 1 the erasure of information in the MD register occurs.

During the second write cycle, number 7 (0111) is rewritten from the four flip-flops of register A into the four ferrite core planes of the 1st byte of the MD register.

The rewriting of the remaining digital bytes and sign code of the number occurs analogously.

The VLS pulse for the 16th byte through the differentiating circuit with $\overline{S16} = 0$ resets flip-flop Z16 into the initial state and turns off the Z counter. A positive voltage drop from output S16 of inverter N87 through gate K141 sets flip-flop R into working order. Sequential pulse S1 through gates K142 and K194, and the differentiating circuits with Z+E8 = 0 reset flip-flops R and VOR into the initial state, and Z16 and set into the working order. Flip-flop B3 remains in running order.

Simultaneously with the setting of the Z16 flip-flop in working order the Z counter is incremented ensuring the display of the dividend. As a result of completing the entry operation and rewriting into the four ferrite core planes of registers MD and MR the arrangement of digital information corresponds to the following table:

<div align="center">

MR - 0000000000001207

MD - 0000000000001207

</div>

III.5.2. Divisor entry.

After loading the divisor the result "=" key is pressed and the corresponding closed keyboard contact, connects a logic 0 signal to the inputs of the keyboard filters L21 and L25, through the functional keyboard encoder diodes. From outputs (=)0 and FU0 logic 0 signals enter the controlling inputs of the differentiating circuits of flip-flops VOR and B4.

Pulse EING through the differentiating circuits set flip-flops B4 and VOR into the working order. After the setting of flip-flop VOR into the working order in the sequence, analogous to the description in section III.2.3, occurs the preparation for completion of the Division operation, I.E. shift and recording of the divisor into register MR in accordance with the assigned degree of accuracy and the Z counter cycle with EING2 = 1. The initial state of flip-flop F2 during the Z counter cycle ensures rewriting of information in register MR → MR. (When flip-flop F2 is located in running order, I.E. The divisor is obtained as a result the Addition or Subtraction operations, the operation of rewriting register AC0 → MR is carried out erasing the information in the AC0 register.) In accordance with the example the divisor remains in the MR register.

The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16} = 0$ resets flip-flop Z16 into the initial state. A positive voltage drop from output S16 of inverter N87 through gate K141 sets flip-flop R into the working order. Sequential pulse S1 through gate K194 and the differentiating circuits resets flip-flop VOR into the initial state and with X+E8=0 sets flip-flop Z16 into the working order. From output $\overline{VOR}$ of inverter N59 a logic 1 signal disables gate K135. From the output of gate K135 a logic 1 signal is fed to the input of the amplifier V567. From output DIV of the signal amplifier a logic 1 through gate D26 is fed to the input of inverter N54. A positive voltage drop from G2 output of the inverter through the differentiating circuits with G220, G240, G280 = 0 set flip-flops Z2, Z4, Z8 and Z16 in working order incrementing the Z counter for control of the 14th byte.

(To the controlling inputs G210, G220, G140, G240, G110, G180, G280 the differentiating circuits logic 0 signals come in the dependence from the position of the decimal point switch). Simultaneously from output DIV a logic 1 signal disables gate K112. As a result at outputs C1 and C4 of inverters N4 and N8 logic 0 signals are generated which disable gates K2 and K24 and disable the operation of the corresponding inhibit driver stages.

The position of the Z counter creates control of the 14th byte. Gate K121 with DIV and SCHREIB = 1 is enabled and ensures operational control of the AC0 register. At outputs MRS and MDS of inverters N29, N38 and N42 logic 0 signals are generated, which are fed to the inputs of gates K6 and K7 and disable the operation of registers MD and MR. Consequently, during the first and second write cycles into the four ferrite core planes of the 14th byte of the AC0 register will be written the rounding off number 5 (0101). The high-order digits of the AC0 register will be used for the record of the decimal digits of the quotient.

The VLS pulse of the 14th byte through gate K187 increments the Z counter for control of the 15th byte.

Simultaneously pulse VLS through gate K171 and the differentiating circuit with F3 = 0 sets flip-flop F4 into the working order. From output $\overline{F4}$ of the inverter N72 a logic 0 signal disables the operation of gate K121. The read and write cycles of the 15th byte of useful work do not occur. (It is absent control of registers). At the inverter outputs of signals AC0, MDS and MRS logic 0 signals are generated, which disable the operation of the corresponding registers.

The VLS pulse of the 15th byte increments the Z counter for control of the 16th byte.

The analysis of the signs of dividend and divisor correspond and occurs in a sequence, analogous to the analysis of the signs of cofactors. Incrementing the Z counter accomplishes in the 16th byte the operations of the analysis of the signs of dividend and divisor.

The first read cycle stores the sign code from the 16th byte of the MD register into the four flip-flops of register A. Operational control of the MD register in the 16th byte with LES and U = 1 ensures the enabled state of gate K105.

During the first write cycle registers MD, MR and AC0 are not governed.

The second read cycle stores the sign code from the 16th byte of the MR register into the four flip-flops of register A. Operational control of the MR register with LES and the V = 1 ensures the enabled state of the AND gates, from the outputs of which logic 0 signals through the OR gates D11 and D15 are fed to the inputs of inverters N29 and N38.

During the second write cycle registers MD, MR and AC0 are not governed. Operational control of the MR register is disabled by the enabled state of gate K93.

A positive voltage drop of the VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter.

A positive voltage drop from the Z16 output through the differentiating circuit with $\overline{R}$ = 0 sets flip-flop F3 into the working order. From output $\overline{F3}$ of inverter N64 a logic 0 signal disables the operation of gates K112, K98 and K157. From F3 output of inverter N65 a logic 1 signal enters the control input of the differentiating circuit and disables the operation of gate K132*. From output F3 of inverter N65 a logic 1 signal disables gate K114. At output SUB of inverter N47 a logic 1 signal is generated, which during the following cycle of the Z counter ensures the completion of the Subtraction operation (0 - MD → MD), after writing the divisor into the ferrite cores of the MD and MR registers the arrangement of digital information corresponds to the following table:

MR 0000000000001200
MD 0000000000001207

III.5.3. Comparison of the absolute values of dividend and divisor (MD → MD), (MR + MD → MD).

The comparison of the absolute values of dividend and divisor is carried out by adding the divisor with the arithmetical Addition of the dividend.

Sequential pulse S1 through gate K185 sets flip-flop Z1 into the working order and increments the Z counter for administration of the 1st byte.

During completion of the Subtraction operation 0 - MD → MD gate K97 is enabled. From the output of gate K97 a logic 1 signal through the gate D15 is fed to inverter N38.

From output MRS of inverters N29 and N38 a logic 0 signal is fed to gate K6 and disables the operation of the MR register.

At completion of the second read and write cycles gate K108 is enabled. From output MDS of inverter N42 a logic 1 signal enters gate K7 and ensures operational control of the MD register.

The Subtraction operation 0 - MD → MD occurs from the 1st through to the 16th bytes inclusively.

Pulse VLS of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. As a result the completion of the Subtraction operation in accordance with the example in register MD will be written the arithmetical addition of dividend 9999999999998793. A positive voltage drop at the S16 output of inverter N87 through gate K144 and the differentiating circuits with VER = 0 and F2 = 0 set flip-flops F1 and F6 into the working order. The setting of the flip-flop F6 into the working order occurs in the case of the equality of information in registers MD and MR.

From the $\overline{F1}$ output of inverter N62 a logic 0 signal enters and disables gate K114. At the ADD1 and ADD outputs of the inverters are generated logic 1 signals, which in the time of the following cycle of the Z counter ensure the completion of the operation of adding the divisor with the arithmetical addition of the dividend (MR + MD → MD). Simultaneously logic 0 signals from outputs $\overline{F1}$ and $\overline{F6}$ of inverters N62 and N76 enter and shut gate K97.

Note –
There does not appear to be any association between output F3 of inverter N65 and the "controlling input and differentiating circuit" of gate K132.

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At output MRS of inverters N29 and N38 is a logic 1 signal generated, which with U = 1 ensures operational control of the MR register.

Control of the MD register occurs with V = 1 through gate K104. The operation of the MR register with the V = 1 is blocked by a logic 1 signal at the MDS entrance of gate D11. Sequential pulse S1 through gate K185 and the differentiating circuit when A1 = 0 sets flip-flop Z1 incrementing the Z counter for completion of the Addition operation of MR + MD → MD.

During the first read cycle number 0 (0000) is stored from the four ferrite core planes of the 1st byte of the MR register into the four flip-flops of register A.

During the first write cycle the number 0 (0000) is rewritten into the four ferrite core planes of the 1st byte of the MR register from the four flip-flops of register A.

During the second read cycle the number 3 (0011) is stored from the four ferrite core planes of the 1st byte of the MD register into the four flip-flops of register A.

During the second write cycle number 3 (0011) is rewritten into the four ferrite core planes of the 1st byte of the MD register from the four flip-flops of register A.

From outputs C1 and C2 of inverters N4 and N6 logic 0 signals enter the inputs and disable the operation of gate K53. From the $\bar{0}$ output of inverter N16 a logic 1 signal enables the operation of gate K180.

The VLS pulse of the 1st byte through gate K180 and the differentiating circuit when S16 = 0 resets flip-flop F6 into the initial state. The initial state of flip-flop F6 is the criterion of the inequality of terms. The addition of the numbers of the remaining bytes is carried out analogously.

During the second read and write cycles the number 9 (1001) is rewritten into the 16th byte of the MD register. From outputs C1 and C8 of inverters N4 and N10 logic 0 signals disable the operation of gate K53. From output $\bar{0}$ of inverter N16 a logic 1 signal enables the operation of gate K174. The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. A positive voltage drop of the S16 output of inverter N87 through gates K169 and K174 and the differentiating circuits with F2 = 0 and ÜBER = 0 set flip-flops F2 and F6 into the working order.

From output F2 of inverter N71 logic 1 signal enables gate K115. At output SUB of inverter N47 a logic 1 signal is generated, which prepares the completion of the Subtraction operation. As a result of the addition of the numbers

$$000000000001200 + 999999999998793 = 999999999999993$$

overflow of the MD register does not occur. The arithmetical Addition, written into register MD, corresponds to the value MD > MR and working order of the flip-flop F6, which accomplishes the Subtraction operation MR - MD → MD and the shift of the information of registers MR and AC0.

III.5.4. Subtraction MR - MD → MD (Complement) and the shift of the information of registers AC0 and MR.

Sequential pulse S1 through gate K185 with A1 = 0 sets flip-flop Z1 into the working order which increments the Z counter for control of the 1st byte.

Operational control of the MR register occurs with U = 1.

Operational control of the MD register occurs with the V = 1 through gate K108.

During the Z counter cycle the Subtraction operation MR - MD → MD is carried out in the sequence, analogous to the description of operation (-AC) - (-MR) → AC.

The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state which turns off the Z counter.

As a result the completion of the Subtraction operation, the number 0000000000001200 - 9999999999999993 = 0000000000001207 the straight number (dividend) is written in register MD.

A positive voltage drop of the output S16 of inverter N87 through gate K149 and the differentiating circuit with ADD = 0 resets flip-flop F1 into the initial state. Sequential pulse S1 through gates K153 and K185, and the differentiating circuits with A1 and Z+E8 = 0 reset flip-flop F2 into the initial state, and flip-flops VER and Z1 into the working order.

During the Z counter cycle operational control of the MR register and shifting of the divisor to one byte to the left occurs. As a result of the shift of information in register MR occurs the Multiplication of a divisor by 10. The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state. A positive voltage drop from output S16 of inverter N87 through gate K144 with F2 = 0 sets flip-flop F1 into the working order. From output F1 of inverter N63 a logic 1 signal disables gate K75. From the output of gate K75 a logic 1 signal is fed to the input of gate D10 which switches the memorising circuit into the working order. From output RÜ of inverter N24 a logic 1 signal enables the operation of gate K195. Sequential pulse S1 through gates K195 and K194 sets flip-flop Z16 into the working order incrementing the Z counter. Gate K122 is enabled, at output AC0 of inverter N45 a logic 1 signal is generated, which ensures operational control of the AC0 register. During the Z counter cycle with RÜ = 1 the shift operation of the rounding off number 5 (0101) to one byte to the right is carried out in the sequence, analogous to the description of the reverse counting of the Z counter. During the decrement of the Z counter from 16th into the 15th byte, at the output S16 of inverter N87 a positive voltage drop through gate K169 and the differentiating circuit with F2 = 0 sets flip-flop F2 into the working order.

After the shift of the 1st byte switching counter Z for control of the 16th byte occurs, I.E. flip-flop Z1 resets into the initial state, Z16 remains in running order. Pulse VLS of the 16th byte through gate K187 set flip-flops Z1, Z2, Z4 and Z8 into the working order and decrements the Z counter for control of the 15th byte.

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A positive voltage drop of the S16 output of inverter N87 through gate K149 and the differentiating circuit with $\overline{VER}$= 0 resets flip-flop F1 into the initial state. From output F1 of inverter N63 a logic 0 signal is fed to the input of gate K77 and switches the memorising circuit into the initial state. After switching of the memorising circuit into the initial state at output RÜ of inverter N24 a logic 0 signal is generated, and at the output $\overline{RÜ}$ of inverter N23 - a logic 1 signal. A positive voltage drop of the VLS pulse of the 15th byte through the differentiating circuit reset flip-flops Z1, Z2, Z4 and Z8 into the initial state and increments the Z counter for control of the 16th byte. From output $\overline{S16}$ of inverter N88 a logic 0 signal enters the control input of the differentiating circuit of flip-flop Z16. The VLS pulse of the 16th byte through the differentiating circuit resets the flip-flop into the initial state and turns off the Z counter. A positive voltage drop from output S16 of inverter N87 through gate K159 and the differentiating circuit with RÜ $\doteq$ 0 resets flip-flop VER into the initial state. From output VER of inverter N68 a logic 0 signal enables gates K177 and K178. A positive voltage drop of the gates outputs through the differentiating circuits reset flip-flops F2, F4 and F6 into the initial state.

III.5.5. Comparison of values after the shift of the information in registers MR, AC (about MD → MD), (MR + MD → MD).

After disconnection by counters flip-flop VER resets into the initial state. From output $\overline{VER}$ of inverter N67 a logic 1 signal disables gate K114. At output SUB of inverter N47 a logic 1 signal is generated, which determines the completion of the Subtraction operation. Sequential pulse S1 through gate K185 and the differentiating circuit when A1 = 0 sets flip-flop Z1 incrementing the Z counter. During the Z counter cycle the Subtraction operation 0 - MD → MD is carried out which occurs in a sequence, analogous to the description in section III.5.3.

$$\begin{array}{r} \_\ 0000000000000000 \\ \underline{0000000000001207} \text{ MD} \\ 9999999999998793 \text{ MD} \end{array}$$

After completion of the Subtraction operation the completion of the addition operation MR + MD → MD occurs.

$$\begin{array}{r} 9999999999998793 \text{ MR} \\ \underline{+\ 0000000000012000} \text{ MD} \\ 0000000000010793 \text{ MD} \end{array}$$

As a result of completing the Addition operation in register MD is written the straight number, flip-flop F6 remains in the initial state, which corresponds to inequality MR > MD, I.E. The number, written into register MR, is more than that written into register MD.

III.5.6. Subtraction (MR - MD → MD) and reverse shift of the information in register MR (divisor).

Completion of the Subtraction operation MR - MD → MD occurs in a sequence, analogous to the description of the Subtraction operation of sections III.3.8. And III.3.9. In this case instead of the AC0 register through gate K108, control of the MD register occurs:

$$\begin{array}{r} \overline{0000000000012000} \text{ MR} \\ \underline{0000000000010793} \text{ MD} \\ 0000000000001207 \text{ MD} \end{array}$$

As a result of completing the Subtraction operation the dividend in register MD will be replaced by the number 0000000000001207. The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16} = 0$ resets flip-flop Z16 into the initial state and turns off the Z counter. A positive voltage drop from output S16 of inverter N87 through gate K149 and the differentiating circuit with ADD = 0 resets flip-flop F1 into the initial state.

Sequential pulse S1 by a positive voltage drop through gate K153 and the differentiating circuits with Z+E8 = 0 resets flip-flop F2 into the initial state and sets VER into the working order. Simultaneously pulse S1 through gate K185 and the differentiating circuit when A1 = 0 sets flip-flop Z1 incrementing the Z counter.

Gate K97 is enabled, at output MRS of inverters N29 and N38 a logic 0 signal is generated. Gates K117 to K124 are disabled, on the outputs AC and AC0 of inverters N44 and N45 logic 0 signals are generated. Gates K101 to K108 are disabled, at output MDS of inverter N42 a logic 0 signal is generated. From outputs AC, AC0, MDS and MRS of the inverters logic 0 signals enter gates K6 to K11 and block the operation of registers AC, AC0, MD and MR. As a result of blocking the registers counter Z is carried out unmarried error with VER = 1.

After setting flip-flop Z16 into the initial state from output S16 of inverter N87 a positive voltage drop through gate K144 and the differentiating circuit with F2 = 0 sets flip-flop F1 into the working order. From output F1 of the inverter a logic 1 signal disables gate K75. From output RÜ of inverter N24 a logic 1 signal prepares gate K195 to decrement the Z counter. Gate K131 is enabled, at output AC0 of inverter N45 a logic 0 signal is generated, which enters gate K8 and disables the operation of the AC0 register.

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At output MRS of inverters (N28)* N38 and (N39)* N29 a logic 1 signal is generated, which ensures control of the MR register.

Sequential pulse S1 through gates K194 and K195 set flip-flop Z16 into the working order hich decrements the Z counter. During switching of the Z counter from the 16th to the 15th byte at output S16 of the inverter N87 is generated a positive voltage drop, which through gate K169 and the differentiating circuit with F2 = 0 sets flip-flop F2 into the working order. During the decrementing count of the Z counter the shift operation of the divisor is carried out to the right by one byte. After reading and writing in the 1st byte flip-flops Z1, Z2, Z4 and Z8 are located in the initial state, with Z16 in running order. The VLS pulse of the 16th byte through gate K187 sets flip-flops Z1, Z2, Z4 and Z8 and decrements the Z counter for control of the 15th byte. At output S16 of inverter N87 is formed a positive voltage drop, which through gate K149 and the differentiating circuit with $\overline{VER}$ = 0 resets flip-flop F1 into the initial state.

From output F1 of inverter N63 a logic 0 signal enables gate K77. From output RÜ of inverter N24 a logic 0 signal disables the operation of the schematics of the reverse counting of the Z counter. The VLS pulse of the 15th byte through gate K187 reset flip-flops Z1, Z2, Z4 and, Z8 into the initial state. The Z16 flip-flop remains set and ensures control of the 16th byte. The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. A positive voltage drop from output S16 of inverter N87 through gates K159 and the differentiating circuit with RÜ = 0 resets flip-flop VER into the initial state. A positive voltage drop from output VER of inverter N68 through gates K173 and K177, and the differentiating circuits resets flip-flop F2 into the initial, and F5 into the working order. The working order of flip-flop F5 indicates the end of the operations of determining the quantity of bytes of the quotient.

III.5.7. Preparatory quotient formation of (0 - MD → MD), (MR + MD → MD).

The preparatory operations for formation of the quotient are carried out in a sequence, analogous to the description the section III.5.5 (0 - MD → MD)

$$
\begin{array}{r}
- 0000000000000000 \\
\underline{0000000000001207} \text{ MD} \\
9999999999998793 \text{ MD}
\end{array}
$$

After the end of the operation and disconnection of the Z counter a positive voltage drop from output S16 of the inverter M87 through gate K144 and the differentiating circuits with F2 = 0 and VER = 0 reset flip-flops F1 and F6 into the working order.

Note -
N38 and N29 listed here are corrections from the original Russian manual in which they were incorrectly listed as N28 and N39, this did not match the circuit and logic drawings.

Sequential pulse S1 through gate K185 and the differentiating circuit with A1 = 0 reset flip-flop Z1 incrementing the Z counter. After incrementing the Z counter the addition operation of the straight number of the divisor with the arithmetical addition of the dividend MR + MD → MD is carried out.

$$
\begin{array}{r}
0000000000001200 \text{ MR} \\
+\ \underline{9999999999998793} \text{ MD} \\
9999999999999993 \text{ MD}
\end{array}
$$

During completion of the Add operation and during the rewriting of the first number into register MD from the $\overline{0}$ output of inverter N16 a logic 1 signal enables the operation of gate K180. The VLS pulse of the 1st byte through gate K180 and the differentiating circuit when S16 = 0 resets flip-flop F6 into the initial state. The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. Simultaneously pulse VLS through gate K174 and the differentiating circuit with ÜBER = 0 resets flip-flop F6 into the working order. The working order of flip-flop F6 determines that the information of the register MD > MR, as a result of this the byte of quotient is added one. After disconnection of the Z counter from output S16 of inverter N87 a positive voltage drop through gate K169 and the differentiating circuit with F2 = 0 resets flip-flop F2 into the working order.

Sequential clock pulses S through gate K91 and the differentiating circuit with $F2$ = 0 resets flip-flop A1 into the working order. From output A1 of inverter N5 a logic 1 signal enters the control input of the differentiating circuit of flip-flop Z1 and disables the setting of flip-flop Z1 into the working order through gate K185.

III.5.8. Quotient formation and comparison of values (MR + MD → MD).

Pulse S1 through gate K194 and the differentiating circuit Z+E8 = 0 resets flip-flop Z16 into the working order and enables the Z counter for of administration of the 16th byte.

Gate K83 is enabled, from output MRS of inverters N29 and N38 a logic 0 signal enters gate K6 and disables the operation of the MR register. Gate K120 with V = 1 is enabled. At output AC0 of inverter N45 a logic 1 signal is generated, which ensures operational control of the AC0 register.

During the first of the read and write cycles control of registers does not occur.

During the second read cycle the number 0 (0000) is stored from the four ferrite core planes of the 16th byte into the four flip-flops of register A.

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During the second write cycle the number 1 (0001) is rewritten from the four flip-flops of the A register the number 1 (0001) is rewritten into the four ferrite core planes of the 16th byte of the AC0 register.

The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter, simultaneously pulse VLS through the differentiating circuit resets flip-flop A1 into the initial state.

From output S16 of inverter N87 a positive voltage drop through gate K176 and the differentiating circuit with ÜBER = 0 resets flip-flop F2 into the initial state.

Sequential pulse S1 through gate K185 and the differentiating circuit with A1 = 0 resets flip-flop Z1 incrementing the Z counter.

During the Z counter cycle the Add operation of MR + MD → MD is carried out

$$
\begin{array}{r}
0000000000001200 \text{ MR} \\
+\ \underline{9999999999999993} \text{ MD} \\
0000000000001193 \text{ MD}
\end{array}
$$

After the record of a number into the 1st byte of the MD register pulse VLS through gate K180 and the differentiating chain with S16 = 0 resets flip-flop F6 into the initial state. In the 16th byte of the MD register is written number 0, therefore, flip-flop F6 do not change initial state. The initial state of flip-flop F6 determines that the information of register MR > MD, as a result this into the byte of quotient one to does not enter. Pulse VLS of the 16th byte by a positive voltage drop through the differentiating chain with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. A positive voltage drop from output S16 of inverter N87 through gate K169 and the differentiating chain with F2 = 0 resets flip-flop F2 into the working order.

III.5.9. Subtraction (MR - MD → MD)
and the shift of registers MD, AC0.

The sequential pulse S1 through gate K185 and differentiating chain with A1 = 0 resets flip-flop Z1 incrementing the Z counter.

Gate K113 it is enabled, on the output SUB of inverter N47 a logic 1 signal is generated, which determines the completion of the operation Subtraction MR - MD > MD

$$
\begin{array}{r}
-\ 0000000000001200 \text{ MR} \\
\underline{0000000000001193} \text{ MD} \\
0000000000000008 \text{ MD}
\end{array}
$$

Completion of the operation occurs in a sequence, analogous to the description in section III.5.6.

The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = by 0 resets flip-flop Z16 into the initial state. A positive voltage drop of the output S16 of inverter N87 through gate K149 and the differentiating circuit with ADD = 0 resets flip-flop F1 into the initial state. Sequential pulse S1 through gate K153 and the differentiating circuits with Z+E8 = 0 reset flip-flops F2 into the initial and VER into the working order. Simultaneously pulse S1 through gate K185 and the differentiating circuit when A1 = 0 resets flip-flop Z1 incrementing the Z counter. Gate K106 is enabled, at output MDS of inverter N42 a logic 1 signal is generated, which enters gate K7 and ensures control of the MD register.

The working order of flip-flop VER carries out the operation of the shift of the remainder of the dividend one byte to the left during the Z counter cycle. As a result of the shift the remainder of the dividend, written into register MD, increases by 10. Pulse VLS through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. A positive voltage drop of the Z16 output of inverter N87 through gate K144 and the differentiating circuit with F2 = 0 resets flip-flop F1 into the working order. Sequential pulse S1 through gate K194 and the differentiating circuit with Z+E8 = 0 resets flip-flop Z16 in working order and it includes counter Z. Gate K122 is enabled, at output AC0 of inverter N45 a logic 1 signal is generated, which enters gate K8 and ensures control of the AC0 register.

During the read cycle from the four ferrite core planes of the 16th byte number 1 (0001) is rewritten into the four flip-flops of register A.

During the write cycle from the four flip-flops of register E number 0 (0000) is rewritten into the four ferrite core planes of the 16th byte register and AC0.

The VLS pulse of the 16th byte through the differentiating circuit resets flip-flop A1 into the initial state and stores number 1 (0001) into the four flip-flops of register E.

Simultaneously pulse VLS through the differentiating circuit resets flip-flop Z16 into the initial state and turns off the Z counter.

A positive voltage drop from output S16 of inverter N87 through gate K169 and the differentiating circuits with $\overline{VER}$ = 0 and F2 = 0 reset flip-flops F2 and Z1 in working order, starting the Z counter.

During the read cycle the number 0 (0000) is stored from the four ferrite core planes of the 1st byte of the AC0 register into the four flip-flops of register A.

During the write cycle the number 1 (0001) is rewritten from the four flip-flops of register E into the four bits of the 1st byte of the AC0 register. The shift of the remaining bytes of the AC0 register occurs in the usual sequence.

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Consequently, as a result of the execution of the shifting operation the number 1 (0001) from the 16th byte is rewritten into the 1st byte of the AC0 register and simultaneously the rounding off number 5 (0101) is shifted one byte to the left, I.E. it is rewritten into the 14th byte. The VLS pulse of the 16th byte resets flip-flop Z16 into the initial state and turns off the Z counter.

A positive voltage drop from output S16 of inverter N87 through gates K149 and K159, the differentiating circuits with $\overline{VER}$ = 0, RÜ = 0 reset flip-flops F1 and VER into the initial state. A positive voltage drop from output VER of inverter N68 through gate K177 resets flip-flop F2 into the initial state.

III.5.10. Comparison of absolute values (0 - MD → MD),
(MR + MD → MD) and the shift of registers MD, AC0.

Sequential pulse S1 through gate K185 and the differentiating circuit when A1 = 0 resets flip-flop Z1 incrementing the Z counter. Gate K114 is enabled, at the SUB output of inverter N47 a logic 1 signal is generated, which determines the completion of the Subtraction operation 0 - MD → MD.

During the first cycle of the Z counter the Subtraction operation is carried out in the usual sequence

$$\begin{array}{r} \underline{-\ 0000000000000000} \\ \underline{\ \ 0000000000000070}\ \text{MD} \quad 0050000000000001\ \text{AC} \\ 9999999999999930\ \text{MD} \end{array}$$

During the second cycle of the Z counter the Addition operation MR + MD → MD is carried out in the usual sequence

$$\begin{array}{r} 0000000000001200\ \text{MR} \\ \underline{+\ 9999999999999930}\ \text{MD} \\ 0000000000001130\ \text{MD} \end{array}$$

As a result of completing the operation flip-flop F6 remains in the initial state.

During the third cycle of the Z counter the Subtraction operation MR - MD → MD is carried out

$$\begin{array}{r} \underline{-\ 0000000000001200}\ \text{MR} \\ \underline{\ \ 0000000000001130}\ \text{MD} \\ 0000000000000070\ \text{MD} \end{array}$$

As a result of completing the Subtraction operation the remainder of the dividend is expressed by the straight number and corresponds to inequality MD < MR. Consequently, the information of registers MD and AC0 must be shifted by one byte to the left.

The following two cycles of the Z counter ensure the shift of the information in the MD and AC0 registers. Consequently, the arrangement of information corresponds to the following record in the four ferrite core planes of the registers:

$$0000000000001200 \quad MR$$

$$0000000000000700 \quad MD$$

$$0500000000000010 \quad AC0$$

After the shift of information in the registers in the sequence, analogous to the description in section III.5.4, occurs the resetting of the corresponding flip-flops into the initial state and the disconnection of the Z counter.

III.5.11. Comparison of values for rounding
(0 - MD → MD) (MR+ MD → MD).

In the sequence, analogous to the description in section III.5.5, the Z counter is started, which carries out the comparison operation of the values in registers MD and MR and the shift of the information in registers MD and AC0.

During the shift of the rounding off number 5 (0101) into the 16th byte of the AC0 register the read cycle stores number 0 (0000) from the four bits of ferrite cores of the 16th byte into the four flip-flops of register A.

The write cycle rewrites the number 5 (0101) into the four ferrite core planes of the 16th byte from the four flip-flops of register E. Gate K49 is disabled with the logic 0 signals of inputs $\overline{E1}$ and $\overline{E4}$. From output E of inverter N14 a logic 1 signal enables the operation of gate K170.

As a result of the shift, the arrangement of the information in the registers corresponds to the following record in the four ferrite core planes of the registers:

$$0000000000001200 \quad MR$$

$$0000000000007000 \quad MD$$

$$5000000000000100 \quad AC0$$

The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16} = 0$ resets flip-flop Z16 into the initial state and turns off the Z counter.

A positive voltage drop of the S16 output of inverter N87 through gates K170, K149 and K159, the differentiating circuits with $\overline{F2} = 0$, $\overline{VER} = 0$, RÜ = 0 resets flip-flop F4 into working, F1 and VER - into the initial state.

A positive voltage drop from output VER of inverter N68 through gate K177 resets flip-flop F2 into the initial state.

The working order of flip-flop F4 determines the completion of the rounding operation of the low order digit of the quotient.

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III.5.12. Comparison of the values (0 - MD →MD), (MR+ MD → MD) and the formation of a low-order quotient digit.

Sequential pulse S1 through gate K185 and the differentiating circuit when A1 = 0 resets flip-flop Z1 into the working order and starts the Z counter for completion of the comparison of values operations. The comparison of values of (0 - MD → MD), (MD + MR → MD) and the formation of the quotient occurs in a sequence, analogous to the description in section III.5.8.

During the first cycle of the Z counter the Subtraction operation 0 - MD → MD is carried out:

$$
\begin{array}{rl}
-\ & 0000000000000000 \\
  & \underline{0000000000007000} \ \ \text{MD} \\
  & 9999999999993000 \ \ \text{MD}
\end{array}
$$

During the second error of the counter the Add operation MR + MD → MD is carried out

$$
\begin{array}{rl}
  & 0000000000001200 \ \ \text{MR} \\
+ & \underline{9999999999993000} \ \ \text{MD} \\
  & 9999999999994200 \ \ \text{MD}
\end{array}
$$

As a result of the comparison of the values of dividend and divisor we obtain MD > MR. During the third cycle of the Z counter into the 16th byte of the AC0 register enters one:

$$6000000000000100 \ \ \text{AC0}$$

During the fourth cycle of the counter the comparison of values is carried out:

$$
\begin{array}{rl}
  & 0000000000001200 \ \ \text{MR} \\
+ & \underline{9999999999994200} \ \ \text{MD} \\
  & 9999999999995400 \ \ \text{MD}
\end{array}
$$

As a result of the comparison of the values of dividend and divisor during the fifth cycle of the Z counter into the 16th byte of the AC0 register enters one:

$$7000000000000100 \ \ \text{AC0}$$

The comparison of values and the formation of the low-order digit of quotient is carried out analogously with the description in section III.5.8.

After the record number 9 (1001) in the 16th byte of the quotient the error is included by counters and the comparison of values, I.E.. is carried out operation MR + MD → MD:

$$
\begin{array}{rl}
  & 0000000000001200 \ \ \text{MR} \\
+ & \underline{9999999999997800} \ \ \text{MD} \\
  & 9999999999999000 \ \ \text{MD} \quad 9000000000000100 \ \ \text{AC0.}
\end{array}
$$

The comparison of the values of dividend and divisor leads to the result MD > MR.

The VLS pulse of the 16th byte through gate K174 and the differentiating chain with ÜBER = 0 sets flip-flop F6 in working order.

From output F6 of inverter N77 a logic 1 signal enables the operation of gate K91.

Simultaneously pulse VLS through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter.

A positive voltage drop from output S16 of inverter N87 through gate K169 and the differentiating chain with F2 = 0 sets flip-flop F2 into the working order.

All the remaining F flip-flops are left in running order after the setting of flip-flop F2. Sequential clock pulses S through gate K91 n the differentiating chain when $\overline{F2}$ = 0 sets flip-flop A1 into the working order.

Sequential pulse S1 through gate K194 and the differentiating circuit with Z+E8 = 0 resets flip-flop Z16 into the working order and starts the Z counter.

Gate K120 with the V = 1 is enabled. At output AC0 of inverter N45 is a logic 1 signal generated, which ensures control of the AC0 register.

During the first of the read and write cycles of control of registers does not occur.

During the second read cycle the number 9 (1001) is stored from the four ferrite core planes of the AC0 register 16th byte into the four flip-flops of register A. After storing the number 9 (1001) into the four flip-flops of register A, addition of 0001 + 1001 is carried out.

As a result of adding 0001 + 1001 and transfer of the overflow bits, a positive voltage drop from output E8 of inverter N21 through gate K64 and the differentiating circuit with U = 0 sets flip-flop ÜBER into the working order. After setting flip-flop ÜBER the number 0 (0000) will be written into the register A flip-flops.

During the second write cycle the number (0000) is rewritten into the four ferrite core planes of the AC0 register 16th from the four flip-flops of register A

Pulse VLS through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. Simultaneously pulse VLS through gate K181 and the differentiating chain with $\overline{F2}$ = 0 resets flip-flop Z1 incrementing the Z counter.

Gate K120 with V = 1 is enabled. At output AC0 of inverter N45 a logic 1 signal is generated, which ensures control of the AC0 register. During the first read cycles of the record of control by registers it does not occur.

During the second read cycle the number 0 (0000) is stored from the four ferrite core planes of the AC0 register 1st byte into the four flip-flops of register A.

A positive voltage drop from output LES of inverter N25 through gates K28 and K68, and the differentiating circuits reset flip-flops ÜBER into the initial state and sets A1 into working order.

During the second write cycle the unit of rounding 1 (0000) is rewritten into the four ferrite core planes of the AC0 register 1st byte from the four flip-flops of register A, The rewriting of the remaining bytes of the AC0 register occurs in the usual sequence.

The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. A positive voltage drop from output S16 of the inverter N87 through gate K176 and the differentiating circuit with ÜBER = 0 resets flip-flop F2 into the initial state.

As a result of rounding the low-order digit in the AC0 register [law is Chen] formation of quotient. The arrangement of information in the AC0 register corresponds to the following record: 0000000000000101.

Sequential pulse S1 through gate K185 and the differentiating circuit with A1 = 0 resets flip-flop Z1 incrementing the Z counter for completion of the comparison of values operation. As a result of the comparison of values we obtain MD < MR:

$$
\begin{array}{ll}
0000000000001200 & MR \\
\underline{+\ 9999099999999000} & MD \\
0000000000000200 & MD
\end{array}
$$

During the transfer of the overflow bits the flip-flop E8 consecutively inverts into the working and initial conditions. A positive voltage drop of the output E8 of inverter N21 through gate K64 and the differentiating circuit with U = 0 sets flip-flop ÜBER into the working order.

The VLS pulse of the 16th byte through gate K180 and the differentiating circuits with $\overline{\text{ÜBER}}$ and $\overline{S16}$ = 0 reset flip-flops F6 and Z16 into the initial state and turns off the Z counter.

A positive voltage drop of the S16 output of inverter N87 through gate K169 and the differentiating chain with F2 = 0 sets flip-flop F2 into the working order. After disconnection of the Z counter the following clock pulse through gate K66 and the differentiating circuit with MUL = 0 resets flip-flop ÜBER into the initial state.

III.5.13. Rewriting a quotient from register AC0 into register MR (AC0 → MR).

After the formation of the quotient flip-flops F1, F2, F3, F4 and F5 are located in the working order and F6 in the initial state.

Sequential pulse S1 through gate K185 and the differentiating circuit when A1 = 0 resets flip-flop Z1 incrementing the Z counter. Gate K119 with U and LES = 1 is enabled. At output AC0 of inverter N45 a logic 1 signal is generated, which ensures control of the AC0 register.

Simultaneously from inverter N45's output AC0 a logic 1 signal enters through the gate D11 to the input of inverter N29. From output MRS of inverters N29 and N38 a logic 0 signal enters gate K6 and disables the operation of the MR register. Control of the operation of the MR register occurs with U and SCHREIB = 1 and V = 1.

During the first read cycle the number 1 (0001) is stored from the 1st byte of the AC0 register into the four flip-flops of register A.

During the first write cycle the number 1 (0001) is rewritten into the four ferrite core planes of the MR register 1st byte from the four flip-flops of register A independently of the previously written information.

During the second read cycle the number of the four bits of the ferrite core of the 1st byte of the MR register in accordance with example 1 (0001) is read without storing into the four flip-flops of register A. Gate K88 is enabled, from the output of inverter N34 a logic 0 signal disables the operation of the read amplifiers.

During the second write cycle from the four flip-flops of register A the number 1 (0001) is rewritten into the four ferrite core planes of the MR register 1st byte. The rewriting of the remaining bytes of quotient is carried out analogously.

The VLS pulse of the 15th byte through gate K187 increments the Z counter for control of the 16th byte. From output S16 of inverter N87 a logic 1 signal disables gate K87. From output HV of inverter N34 a logic 0 signal disables the operation of the read amplifiers.

During the first read cycle the number of the four ferrite core planes of the 16th byte of the AC0 register in accordance with example to 0 (0000) is read without storing into four flip-flops of the A register (I.E. The information of four bits is erased).

During the second write cycle from the four flip-flops of register A the number 0 (0000) is rewritten into the MR register 16th byte.

The VLS pulse of the 16th byte through the differentiating chain with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. A positive voltage drop of the output S16 of inverter N87 through gate K133 and the differentiating circuit with F6 = 0 resets flip-flop B3 into the initial state.

From the B3 output of the flip-flop a logic 0 signal enables gate K135. A positive voltage drop of the DIV output of amplifier V567 through the differentiating circuit resets flip-flop F2 into the initial state. Sequential clock pulses S through gate K134 and the differentiating chain with $\overline{R}$ = 0 resets flip-flop B4 into the initial state. Following pulse S1 through gate K142 and the differentiating chain with Z+E8 = 0 resets flip-flop R into the initial state. Simultaneously pulse S1 through gate K194 and the differentiating circuit with Z+E8 = 0 resets flip-flop Z16 into the working order incrementing the Z counter. A positive voltage drop from output K the inverter N58 through the differentiating circuits reset flip-flops F1, F3, F4 and, F5 into the initial state.

Table of the sequence of activity of the functional circuit elements
for the general case of Division, with a numerical example.

№ of the opera-tion	Operation carried out	Operation selection for result	State and transition of the control flip-flops F1 F2 F3 F4 F5 F6						Notes	Registers		
										MD	MR	AC
1	2	3	4	5	6	7	8	9	10	11	12	13
	Dividend entry									000…01207	000…01207	0000…0000
	Divisor entry									000…01207	000…01200	0000…0000
	Equals key									000…01207	000…01200	0000…0000
1	Record of rounding off number 5 into 16th byte of register AC0. Analysis of the signs of dividend and divisor.	SUB = 1. Operation № 2 is carried out.	0/0	0/0	0/1	0/1	0/0	0/0	According to an example the 14th byte is selected. At output DIV a logic 1 signal is generated. Inversion of flip-flops; F4 - through K171; F3 - through the differentiation chain, with $\overline{R}$ =0, SUB=1 - through gate K114	000…01207	000…01200	0050…0000
2	Preparation, for the comparison of the absolute values of dividend and divisor.	Operation № 3 is carried out.	0/1	0/0	1/1	1/1	0/0	0/1	F1, F6 - through gate K144	999…98793	000…1200	0050…0000

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№												
3	Comparison of the absolute values of dividend and divisor. MR + MD→ MD	MD→MR, operation № 4- 8 are carried out. With MD < MR operation № 28 is carried out.	0/0	0/1	0/0	0/0	0/0	1/0 (1)	F2 = 1 through K169; F6 - into the initial state through K180 and into working order through K174 with MD > MR. SUB = 1 - through K115	999…99993 MD>MR	000…01200	0050…0000
4	Complement of dividend. MR - MD → MD	Operation № 5 is carried out.	1/0	1/0	1/1	1/1	0/0	1/1	F1, F2 through K149 K153 VER = 1 through K153	000…01207	000…1200	0050…0000
5	Shift MR one byte to the left	Operation № 6 is carried out.	0/1	0/0	1/1	1/1	0/0	0/0	F1 - through K144	000…01207	00…12000	0050…0000
6	Shift AC0 one byte to the right	Operation № 7 is carried out. During record by 5 into the 1st byte AC0 is carried out operation № 29.	1/0	1/0	1/1	1/0	0/0	1/0	F1 - through K149, F4 - through K178, F6 - through K177, VER=0 - through K159, F2=0 - through K177 SUB= 1- through K114	000…01207	00…012000	00050…000
7	Preparation for the completion of the operation of the comparison of absolute values. 0 - MD→MD	Operation № 8 is carried out.	0/1	0/0	1/1	0/0	0/0	0/1	F1, F6 - through K144	999…8793	000…12000	00050…000

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№ of the operation	Operation carried out	Operation selection for result	State and transition of the control flip-flops F1 F2 F3 F4 F5 F6						Notes	Registers		
										MD	MR	AC
1	2	3	4	5	6	7	8	9	10	11	12	13
8	Comparison of the absolute values of dividend and divisor. MR + MD→ MD	MD > MR, operations № 4 - 8 are carried out. With MD < MR operations № 9 – 13 are carried out.	1/1	0/1	1/1	0/0	0/0	1/1 (0)	F2 - through gate K169, F6 - into the initial state through K180, with MD < MR. SUB=1- through K113	000…10973 MD < MR	000…12000	00050…000
9	Complement of the dividend MR – MD→ MD	Operation № 10 is carried out.	1/0	1/0	1/1	0/0	0/0	0/0	F1 – through K149, F2 – through K153	000…01207	000…12000	00050…000
10	Direct idle miscalcula- tion of the Z counter	Operation № 11 is carried out	0/1	0/0	1/1	0/0	0/0	0/0	F1 – through K144	000…01207	000…12000	00050…000
11	Shift MR one byte	Operation № 12 is carried out	1/0	1/0	1/1	0/0	0/1	0/0	F1 – through K149, F2 – through K169 and K177, E5 – through K173	000…01207	000…1200	00050…000
12	Preparation for the formation of quotient.	Operation № 13 is carried out	0/1	0/0	1/1	0/0	1/1	0/1	F1, F6– through K144	999…8793	000…1200	00050…000

	0 - MD → MD										
13	Comparison of the absolute values MR + MD → MD	MD > MR, operation № 14 is carried out. With MD < MR, operations № 16 – 18 are carried out.	1/1	0/1	1/1	0/0	1/1	1/0 (0)	F2 – through K169. With MD ≥ MR F6 remains set through K174	999…9993 MD > MR	000…1200	00050…000
14	Record 0001 into 16th byte of AC0	Operation № 15 is carried out.	1/1	1/0	1/1	0/0	1/1	1/1	F2 – through K176	999…9993	000…1200	1050…000
15	Comparison of the absolute values. MR + MD → MD	MD ≤ MR, operation № 15 is carried out. With MD < MR, operations № 16 – 18 are carried out	1/1	1/0	1/1	0/0	1/1	1/1 (0)	F2 – through K169	999…1193	000…1200	1005…000
16	Complement of the dividend. MR – MD → MD	Operation № 16 is carried out.	1/0	1/0	1/1	0/0	1/1	0/0	F1 through K149, through K153	000…0007	000…1200	1005…000
17	Shift MD one byte to the left	Operation № 18 is carried out.	0/1	0/0	1/1	0/0	1/1	0/0	F1 – through K144	000…0070	000…1200	1005…000

№ of the opera-tion	Operation carried out	Operation selection for result	State and transition of the control flip-flops F1 F2 F3 F4 F5 F6						Notes	Registers		
										MD	MR	AC
1	2	3	4	5	6	7	8	9	10	11	12	13
18	Shift AC0 one byte to the left	With record by 5 into the 16th byte AC0 is performed the operation № 2. In the general case of operation No 19, 20	1/0	1/0	1/1	0/0	0/0	1/1	F2 - through K169 it is working, through K177 - into the initial state, F1 through K149	000…0070	000…1200	0050…001
19	Preparation for the comparison of absolute values. 0 - MD → MD	Operation № 20 is carried out.	0/1	0/0	1/1	0/0	1/1	0/1	F1, F6 - through K144	999…9930	000…1200	0050…001
20	Comparison of absolute values MR + MD → MD	With MD < MR operations № 16-20 are carried out. With MD > MR operations № 16, 17 are carried out	1/1	0/1	1/1	0/0	1/1	1/0	F2 - through K169, F6 - into the initial state with MD < MR	000…1130 MD < MR	000…1200	0050…001
16	With MD < MR operations № 16-20 are repeated. Complement									000…0070	000…1200	0050…001

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	MR - MD → MD											
17	Shift MD one byte to the left.									00…00700	000…1200	0050…001
18	Shift AC0 one byte to the left.									0…00700	000…1200	0500…010
19	Preparation for the comparison of absolute values. 0 - MD → MD.									99…99300	000…1200	0500…010
20	Comparison of the absolute values. MR + MD →MD.	With MD > MR operations № 16-20 are carried out. With MD< MR operation № 16, 17 are carried out.								00…00500 MD < MR	000…1200	0500…010
16	With MD < MR operations No 16, 17 are repeated. Complement MR - MD → MD									00…0700	000…1200	0500…010
17	Shift MD one byte to the left		0/1	0/0	1/1	0/0	1/1	0/0	The state of flip-flops is analogous with operation № 17	0…007000	000…1200	0500…010

№ of the opera-tion	Operation carried out	Operation selection for result	State and transition of the control flip-flops F1 F2 F3 F4 F5 F6						Notes	Registers		
										MD	MR	AC
1	2	3	4	5	6	7	8	9	10	11	12	13
21	Shift AC0 one byte to the left		1/0	1/0	0/0	0/1	1/1	0/0	F2 - through K169 into working order, through K177 - into the initial state, F1 - through K149, F4 - through K170	0…007000	000…1200	5000…100
22	Preparation for the comparison of absolute values. 0 – MD → MD		0/1	0/0	1/1	1/1	1/1	0/1	F1, F6 – through K144	9…993000	000…1200	5000…100
23	Comparison of the absolute values MR + MD → MD	With MD > MR operation № 14 is carried out. With MD < MR operations № 16-18 are carried out.	1/1	0/1	1/1	1/1	1/1	1/1	F2 – through K169 MD > MR	9…994200	000…1200	5000…100
24	Write 0001 into the 16th byte of AC0	Operation № 23 is carried out.	1/1	1/0	1/1	1/1	1/1	1/1	F2 – through K176	9…994200	000…1200	6000…100
23	Comparison of the values	With MD >MR operation № 24	1/1	0/1	1/1	1/1	1/1	1/1	F2 – through K169	9…995400	000…1200	6000…100

	MR + MD → MD	is carried out.										
		With MD < MR operations № 16 - 18 are carried out										
24	Write 0001 into the 16th byte of AC0	Operation № 23 is carried out.	1/1	1/0	1/1	1/1	1/1	1/1	F2 - through K176	9…995400	000…1200	7000…100
23	Comparison of values. MR + MD → MD	With MD > MR operation № 24 is carried out. With MD < MR operations № 16 - 18 are carried out	1/1	0/1	1/1	1/1	1/1	1/1	F2 - through K169	9…996600	000…1200	7000…100
24	Record by 0001 into the 16th byte of AC0	Operation № 23 is carried out	1/1	1/0	1/1	1/1	1/1	1/1	F2 - through K176	9…996600	000…1200	8000…100
23	Comparison of values. MR + MD → MD	With MD > MR operation № 24 is carried out. With MR < MR operations № 16 - 18 are carried out.	1/1	0/1	1/1	1/1	1/1	1/1	F2 - through K169	99…997800	000…1200	8000…100
24	Write 0001 into the 16th byte of AC0	Operation № 23 is carried out.	1/1	1/0	1/1	1/1	1/1	1/1	F2 - through K176	99…997800	000…1200	9000…100

№ of the opera-tion	Operation carried out	Operation selection for result	State and transition of the control flip-flops F1 F2 F3 F4 F5 F6						Notes	Registers		
										MD	MR	AC
1	2	3	4	5	6	7	8	9	10	11	12	13
23	Comparison of the values of MR - MD → MD	With MD > MR. Operation №24 is carried out. When MD < MR operations № 16 - 18 are carried out.	1/1	0/1	1/1	1/1	1/1	1/1	F2 - through K176	99…999000	000…1200	9000…100
24	Write 0001 in the 16th byte of AC0	Operation № 25 is carried out.	1/1	1/1	1/1	1/1	1/1	1/1		99…999000	000…1200	9000…100
25	Write 0001 into the 16th byte of AC0		1/1	1/0	1/1	1/1	1/1	1/1	F2 - through K176	99…99900	000…1200	000…101
23	Comparison of the values of MR - MD → MD	With MD > MR. Operation №24 is carried out. MD < MR, № 26 is carried out.	1/1	0/1	1/1	1/1	1/1	1/1	F2 - through K169, F6 - into the initial state through K180. With MD<MR	00…000200	000…1200	0000…10
26	Shift of quotient fromAC0 in MR	Operation № 27 is carried out.	1/0	1/0	1/0	1/0	1/0	0/0	Initial state through K142, F1, F3 - F6 through the R/C chains from the positive drop R of inverter N58. F2 from DIV=0			

When the quotient has a "minus" sign, flip-flop MZ is located in running order. From output S16 of inverter N87 a logic 1 signal disables gate K152. At output C1 of inverter N4 a logic 0 signal is generated, which ensures the "minus" sign code 0001 is written during the second write cycle into the 16th byte of the MR register. The VLS pulse of the 16th byte through the differentiating circuit with $\overline{S16}$ = 0 resets flip-flop Z16 into the initial state and turns off the Z counter. Sequential pulse S1 through gate K186 and the differentiating circuit with X = 0 sets flip-flop Z1 in working order and increments the Z counter for display of the quotient.

III 5.14. Exceeding register length with Division.

Exceeding the register length during formation of the quotient occurs when the quotient exceeds the permissible 15th byte limit of the register length. A quantity of bytes of quotient is determined to the beginning of its formation via the comparison of the values of dividend and divisor. The result of comparison MD > MR ensures the shift of the information of registers MR one byte to the left, AC0 - one byte to the right. Consequently, rounding off number 5 (0101) is shifted one byte to the right. A different order of magnitudes of dividend and divisor leads to the sequential execution of the operations of the comparison of values and shift of the information of registers MR and AC0.

As a result of the specific number of shifts the rounding off number 5 (0101) is shifted into the first byte of the AC0 register. After shift into the 1st digit number 5 (0101) in the usual sequence the comparison of values occurs and the start of the shift of the information of the AC0 register with MD > MR.

During the shift of information in the AC0 register the rounding off number 5 (0101) is stored into the four flip-flops of register A. The VLS pulse of the 1st byte through gate K186 decrements the Z counter control of the 16th byte and simultaneously stores the number 5 (0101) from the four flip-flops of register A into the four flip-flops of register E. Flip-flops E1 and E4 invert into the working order. From outputs $\overline{E1}$ and $\overline{E4}$ logic 0 signals enable gate K49. From output E of inverter N14 a logic 1 signal disables gate K165. From the output of gate K165 a logic 1 signal enters through gate D25 to the input of inverter N69. From the output of inverter N69 a logic 0 signal disables the operation of gate K162. From output MS of the gate a logic 0 signal is fed to the differentiating chain input and disables the operation of the memory timing monostable for the shaping of pulses t and $\overline{t}$.

During the completion of operation №27 the sign is written into the 16th byte of the MR register; no operation №28 is carried out with the condition MV < MR in the operation №3, after the comparison of values is carried out shift MD one byte to the left and reverses the Z counter cycle. In the event of an overflow the operation is stopped (operation №29).

Note –
Operations 27-29 mentioned above are missing from the sequence table above, pages 174-182.

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CHAPTER IV

Maintenance.

The basis of construction of this computer is the principle of assembling separate units, constructed in essence on the elements, used in the pulse technique. In comparison with electromechanical models of computers, the absence of the wear of mechanical components and other units completely changes the nature of maintenance. The need for regular preventive inspection, lubricant and replacing of worn components and mechanical units is eliminated.

In normal usage the machine must be protected from dampness and dust. The removal of dust from the current-carrying surfaces of the circuit boards and units is effected by a soft hair brush, approximately 1- 2 times during the year depending on the operating conditions.

After the end of work the machine should be covered with a special case and the mains plug removed from the mains voltage supply network.

When in the process of completing arithmetic operations or other calculations the result does not appear to correspond to actual value and deviations appear through the fault of the machine, it is necessary via analysis of the operation of the functional diagrams to determine the emergent malfunction.

The arbitrary symbol in the form of common fraction at inputs and outputs of each element of the functional diagram is determined thus: the numerator of fraction - number of the joint contact, the denominator of fraction - number of the board assembly or joint.

From the overall functional diagram one should turn to the functional diagrams of the boards (Fig. 34 - 45), which provide the possibility of a more detailed analysis.

When as a result the analysis of functional diagram it is impossible to reach the desired result, for determining the emergent malfunction, the display panel of an electronic invoice machine "Soemtron-381" of the type 8601 is connected.

The arrangement of boards in the arithmetic-logic unit depends on the date of manufacture of the machine and can have a normal or reversed sequence, I.E. board 1 or 12 can be the first board from the right side of the arithmetic-logic unit.

IV.1. Prufgerat panel connection.

1) Remove the upper rear cover of the machine.
2) Remove the connecting plug from joint V7.
3) Connecting the display panel through the contacts of joints V7 and, V8.
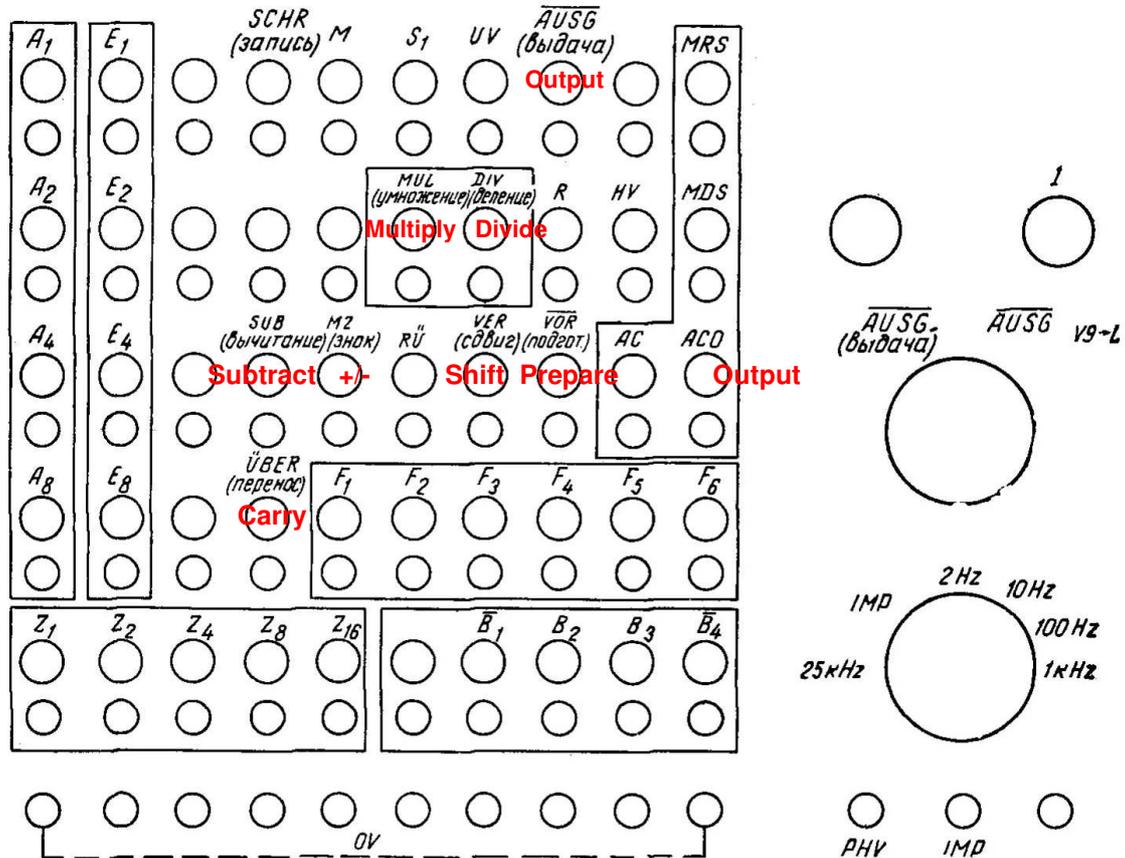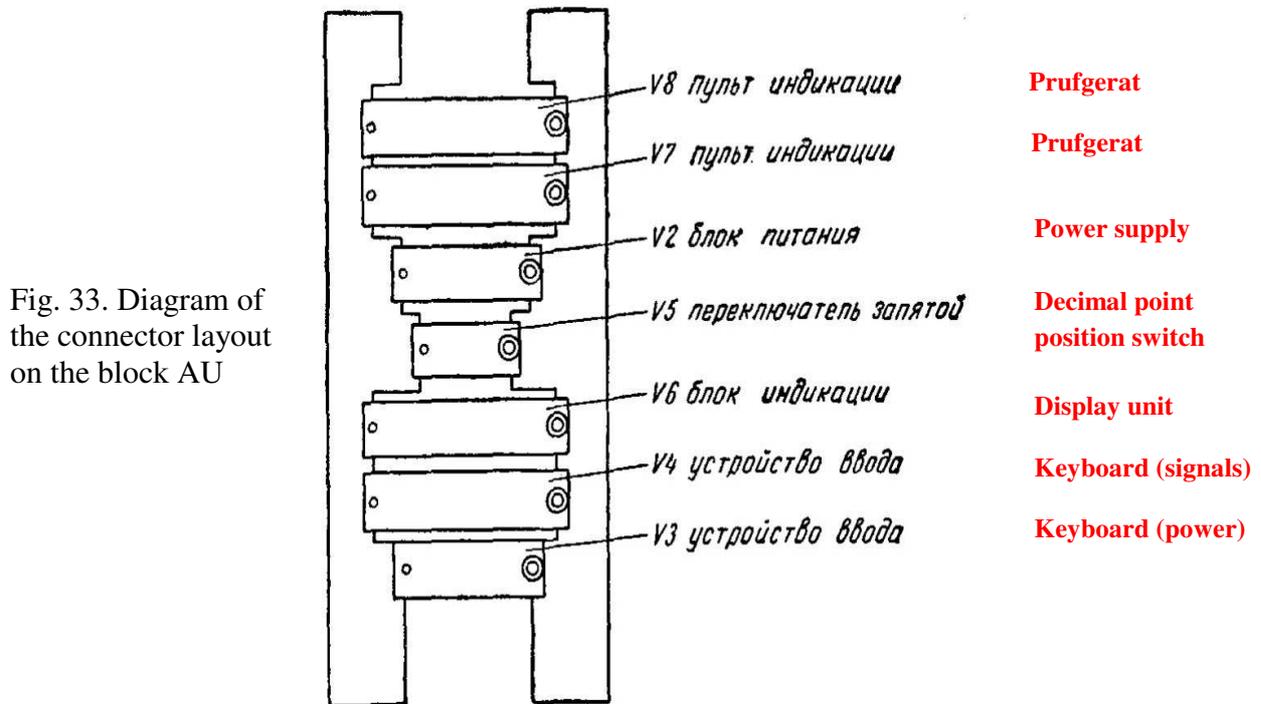4) Fit the display legend to the indicator panel (Fig. 32).

Fig. 32. Prufgerat panel legend.

5) Connect the mains supply voltage to the machine and the display panel.
6) Set the indicator panel switch to the $\overline{\text{AUSG}}$ (0 - 9) position (Fig. 32).
7) Turn on the EIN-AUS toggle switch of the display panel to the position EIN (switched).
8) Turning the switch EIN - AUS to connect the mains voltage to the schematic of machine.
9) Press the Lö key to reset the machine and the indicator panel for checking the completion of arithmetic operations.

Checking the sequential switching of the elements in the electronic circuit with completion of arithmetic operations is produced by visual observation of the appropriate signal lamps of the display panel.

Zak. 794

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A illuminated signal lamp corresponds to a logic 1 signal at the output of the equivalent component of an electronic circuit.

Analog sockets serve for the connection of an oscilloscope to the display panel. Use of the digital and functional keyboard for checking the switching of elements of the machine and completion of arithmetic operations should be produced in the sequence, analogous to the description of chapter 1.

Fig. 33. Diagram of the connector layout on the block AU

V8 пульт индикации — **Prufgerat**

V7 пульт. индикации — **Prufgerat**

V2 блок питания — **Power supply**

V5 переключатель запятой — **Decimal point position switch**

V6 блок индикации — **Display unit**

V4 устройство ввода — **Keyboard (signals)**

V3 устройство ввода — **Keyboard (power)**

During operation with the diagnostic display panel it is necessary to consider the following conditions:

A digital key should be held in the switched position until it is shown on the corresponding indicator lights of the four flip-flops of register E.

Functional keys should be held in the switched position until it is shown that the indicator lights of the Z counter are turned off. The completion of the corresponding operation will occur after the release of the pressed key if are preliminarily sealed (closed ?) the diodes of the inputs Z/0 and FU0 Schmitt flip-flop.

With the presence of the diodes at the entrances of the Schmitt trigger indicated the start of operation occurs in 10ms independent of the time of the release of key.
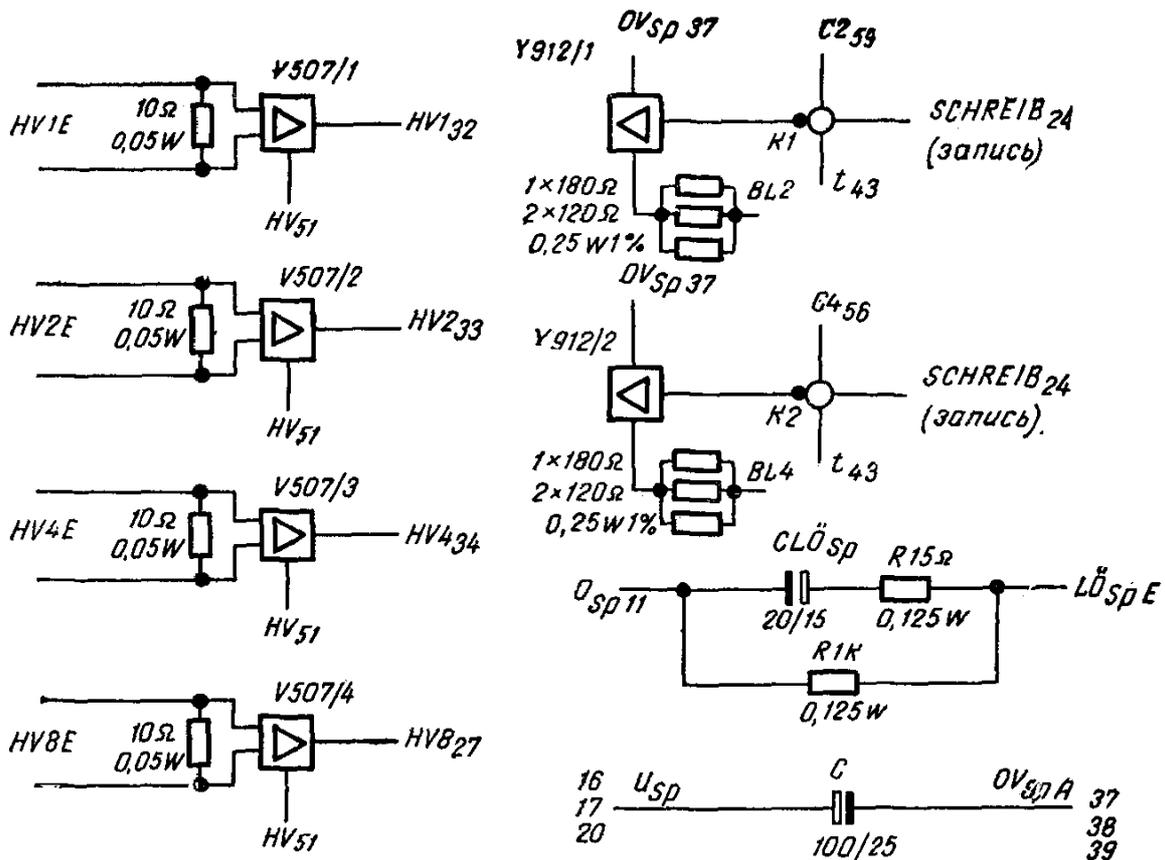
Operational speed of the elements of the network of the machine depends on a master oscillator in the display panel with switched ranges giving frequencies of 2 Hz, 10 Hz, 100 Hz, 1 kHz and 25 kHz.

In the switch position IMP and with each press of the IMP push button generates one clock pulse S, I.E. The possibility of manual control is created.

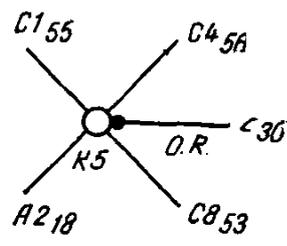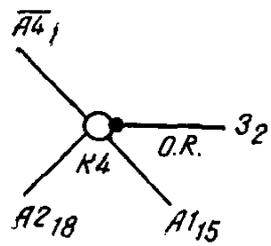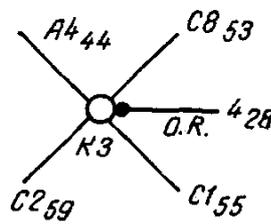## IV.2.	Connection tables and Signal names.

Board 1

Number	Signal name	Addresses of the field joints			
1	$\overline{A4}$	3/3			
2	3	5/12			
3	$\overline{Z8L}$	3/2			
4	Z8S	4/2			
5	Z8L	5/2			
6	S4S	6/2			
7	S4L	7/2			
8	$\overline{S4L}$	8/2			
10	$\overline{S4S}$	10/2			
11	Lö$_{SP}$		32V4		
15	A1	16/3/4; 20/8; 19/10			2V8
16	-U$_{SP}$	20/2	9, 10V2		
17	-U$_{SP}$	20/2	9, 10V2		
18	A2	19/3; 4	12V8		
19	ZMD	19/2			
20	-U$_{SP}$	20/2	9, 10V2		
21	ZAC3	21/2			
22	ZAC0	22/2			
23	ZAC1	23/2			
24	SCHR	24/2; 25/5/6			5V8
25	ZMR	25/2			
26	ZAC2	26/2			
27	HV8	25/3			
28	4	28/12			
30	2	29/12			
32	HV1	32/3			
33	HV2	33/3			
34	HV4	34/3			
37	O$_{VSP}$A	37/2	17V3		
38	O$_{VSP}$A	38/2	18V3		
39	O$_{VSP}$A	39/2	19V3		
40	$\overline{Z8S}$	40/2			
41	SS3	41/2			
42	$\overline{t}$	42/2			
43	t	43/2			
44	A4	44/3/4; 45/8	22V8		
45	BL8	45/2			
46	BL1	46/2			
47	SS2	47/2			
48	$\overline{A8}$	48/3; 34/9			
49	SS4	49/2			
50	SS1	50/2			
51	HV	51/5	20V8		
53	C8	53/2; 54/3; 53/4			
55	C1	56/2/3/4			
56	C4	58/3; 57/4			
59	C2	59/3/4			
60	0V	60/1-12	11, 12V2: 5, 6V3;	1V8	
61	+U$_{P}$	61/1-12	13V2;	21V7	
62	-U$_{N}$	62/1-12	14, 15V2; 29V6;	20V7	

Fig. 34. Functional diagram of board 1.

Board 2

Number	Signal name	Addresses of the field joints	
1	K162	1/9	
2	MDS	2/5; 1/6	21V8
3	$\overline{Z8L}$	3/1	
4	Z8S	4/1	
5	Z8L	5/1	
6	S4S	6/1	
7	S4L	7/1	
8	$\overline{S4I}$	8/1	
9	$\overline{ST}$	10/5/6/7/8; 13/9	
10	$\overline{S4S}$	10/1	
11	F5	12/4; 15/5/6/7; 14/9	7V7
12	Z4	13/5; 12/10; 11/11	11V7
13	$\overline{F4}$	14/3/6; 15/9	
14	F4	18/6; 19/7; 18/9	6V7
15	LES	15/4; 16/5/6	
16	-Usp	20/1	9, 10V2
17	-Usp	20/1	9, 10V2
18	Z8	23/5/7; 21/10; 23/11	12V7
19	ZMD	19/1	
20	-Usp	20/1	9, 10V2
21	ZAC3	21/1	
22	ZAC0	22/1	
23	ZAC1	23/1	
24	SCHR	24/1; 25/5/6	5V8
25	ZMR	25/1	
26	ZAC2	26/1	
27	$\overline{F5}$	11/3; 12/5/6/9	
29	$\overline{Z8}$	22/10; 28/11	
30	$\overline{Z4}$	23/10; 29/11	
31	AC	30/5; 31/6	30V8
32	AC0	32/5/6	31V8
33	MRS	35/5/6	11V8
36	S1	36/4; 35/5/7; 348/10	7V8
37	0VspA	37/1	17V3
38	0VspA	38/1	18V3
39	0VspA	39/1	19V3
40	$\overline{Z8S}$	40/1	
41	SS3	41/1	
42	$\overline{t}$	41/5	
43	t	43/1	
45	BL8	45/1	
46	BL1	46/1	
47	SS2	47/1	
49	SS4	49/1	
50	SS1	50/1	
53	C8	53/1; 54/3; 53/4	
54	Z1	55/5; 48/10/11	9V7
56	C1	55/1; 56/3/4	

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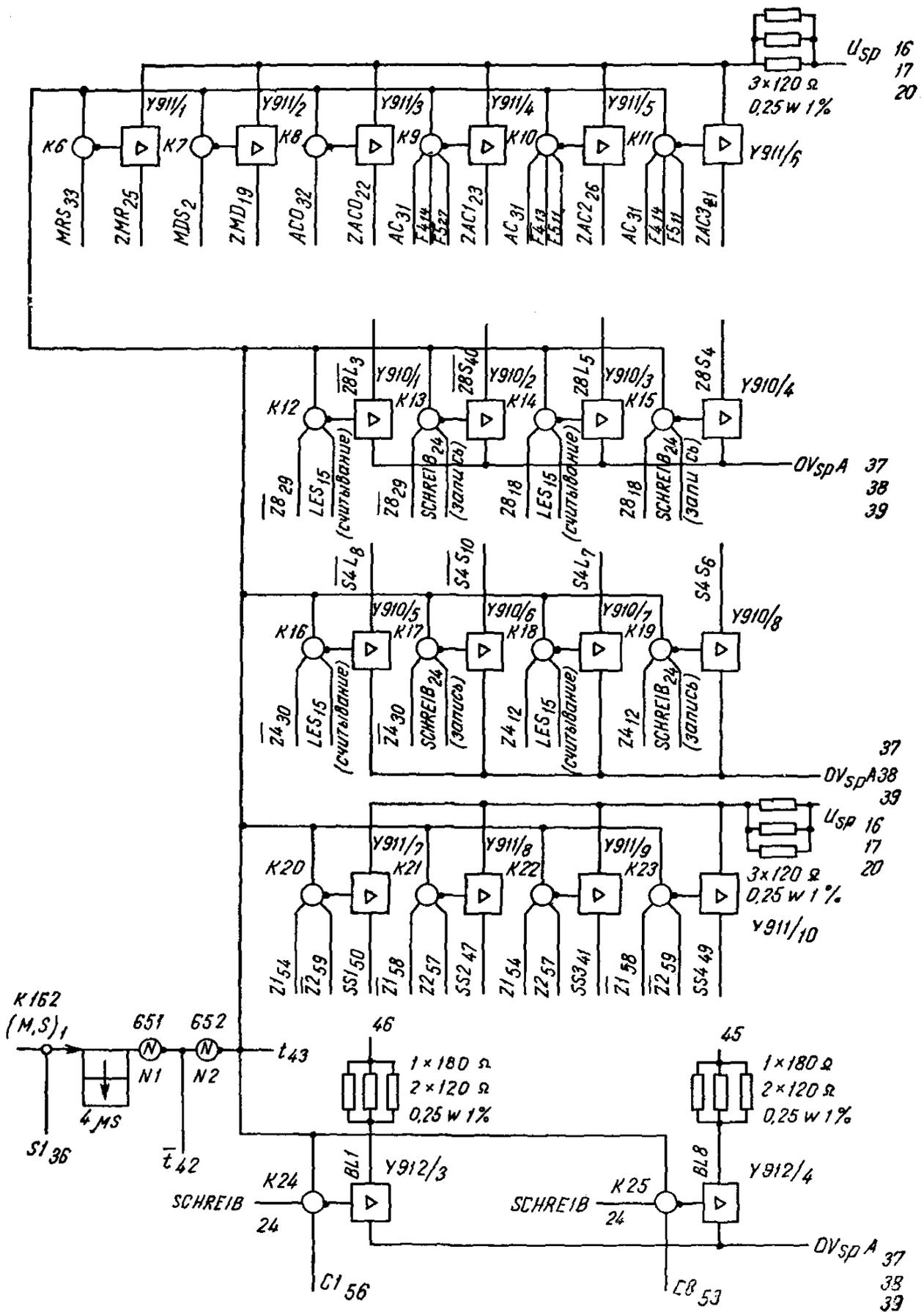
Fig. 35. Functional diagram of board 2.

Number	Signal name	Addresses of the field joints		
57	Z2	59/5; 54/10; 52/11		10V7
58	$\overline{Z1}$	49/10/11		
59	$\overline{\overline{Z2}}$	55/10; 51/11		
60	0V	60/1-12	11,12V2; 5,6V3;	1V8
61	+U$_\text{p}$	61/1-12	13V2;	21V7
62	-U$_\text{N}$	62/1-12	14,15V2; 29V6;	20V7

Board 3

Number	Signal name	Addresses of the field joints	
1	7	1/12	
2	8	2/12	
3	$\overline{A4}$	1/1	
4	$\overline{B3}$	6/7	
5	9	5/4; 6/12	
7	VLS	7/4/5; 6/8/9/10	
8	F3	8/5/6/7/8/9	5V7
9	MUL	10/4; 11/5/6/7/8/9/10	17V8
11	$\overline{F5}$	27/2; 12/5/6/9	
14	$\overline{F4}$	13/2; 14/6; 15/9	
15	K28	14/4	
16	A1	15/1; 16/4; 20/8; 19/10	2V8
19	A2	18/1/4	12V8
20	K112	20/6	
21	E2	23/4	13V8
22	SvM	22/6	
24	VER	26/4/5/6/7/8/9/10	
25	HV8	27/1	
26	A8	27/4	32V8
27	$\overline{B4}$	27/6/7/9/10	18V7
28	MZ	29/8	
29	E8	30/4	1V7
30	5	30/12	
31	6	31/12	
32	HV1	32/1	
33	HV2	33/1	
34	HV4	34/1	
35	E1	35/4	3V8
37	V	36/5; 35/6	15V8
39	A1F	39/4	
40	VER	41/4; 40/5; 39/6; 40/8; 41/9	28V8
41	A8F	42/4; 41/7	
42	A2F	43/4; 41/6	
43	$\overline{F2}$	43/6; 44/9; 43/10	
44	A4	44/1/4; 45/8	22V8
45	K91	46/5	

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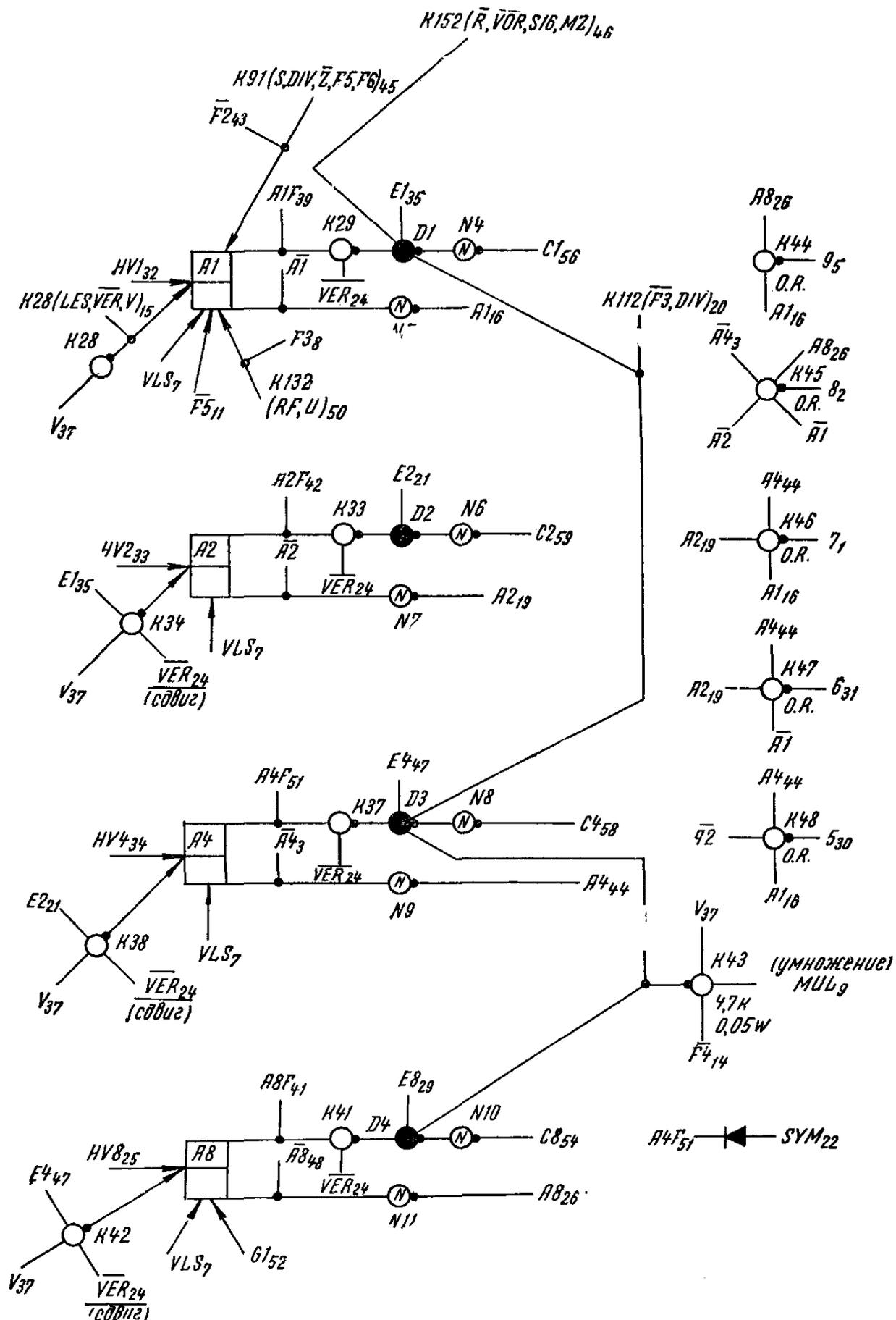
Fig. 36. Functional diagram of board 3.

Number	Signal name	Addresses of the field joints		
46	K152	48/8		
47	E4	49/4		23V8
48	$\overline{A8}$	48/1; 34/9		
49	$\overline{B2}$	49/7		
50	K132	51/7		
51	A4F	51/4		
52	G1	52/4/8/10		
53	$\overline{F6}$	55/6; 56/7; 54/8; 53/9		
54	C8	53/1/2/4		
56	C1	55/1; 56/2/4		
57	$\overline{B1}$	57/6/7		15V7
58	C4	56/1; 57/4		
59	C2	59/1/4		
60	0V	60/1-12	11,12V2; 5,6V3;	1V8
61	$+U_p$	61/1-12	13V2;	21V7
62	$-U_N$	62/1-12	14,15V2; 29V6;	20V7

Board 4

Number	Signal name	Addresses of the field joints	
1	K65	2/7; 1/8	
2	AU	1/5; 16/12	
3	ADD1	2/6	
4	ADD	3/6/8/9/10	
5	9	5/3; 6/12	
7	VLS	7/3/5; 6/8/9/10	
8	R	7/6/7/8/9/10	19V8
9	$\overline{MZ}$	9/8; 10/9	26V8
10	MUL	9/3; 11/5/6/7/8/9/10	17V8
11	Z/20	22/12	
12	F5	11/2; 15/5/6/7; 14/9	7V7
13	U	14/5; 13/6/7/8	
14	K28	15/3	
15	LES	15/2; 16/5/6	
16	A1	15/1; 16/3; 20/8; 19/10	2V8
17	X	17/5; 16/8/9; 13/10	
18	A2	18/1; 19/3	12V8
19	K66	20/5	
20	S	19/5/6; 20/7; 19/8; 20/9	
21	EING	21/7; 22/8; 22/9; 20/10	
22	$\overline{Z}$	22/5/7; 21/8; 22/9; 20/10	
23	E2	21/3	13V8
25	$\overline{MUL}$	25/7/9/10	
26	$\overline{VER}$	24/3; 26/5/6/7/8/9/10	
27	A8	26/3	32V8

Fig. 37. Functional diagram of board 4.

Number	Signal name	Addresses of the field joints		
28	$\overline{R}$	27/5; 28/7; 27/8; 28/9/10		
29	X	29/5; 30/6/7/8; 54/4		
30	E8	29/3		1V7
31	EÜBER E̅ÜBER̅	31/9		
32	ÜBER $\overline{\text{ÜBER}}$	32/8/9		
33	Z+E8	33/7/8/9; 32/10		
34	G2	34/7; 33/10		
35	E1	35/3		3V8
36	S1	36/2; 35/5/7; 34/8/10		7V8
37	Z/40	35/12		
38	Z/80	34/12		
39	A1F	39/3		
40	I	41/12		
41	VER	40/3/5/; 39/6; 40/8; 41/9		28V8
42	A8F	41/3/7		
43	A2F	42/3; 41/6		
44	A4	44/1/3; 45/8		22V8
47	ÜBER	46/8; 47/9; 46/10		2V7
48	0	49/9; 40/12		
49	E4	47/3		23V8
50	Z/10	42/12		
51	A4F	51/3		
52	G1	52/3/8/10		
53	C8	53/1/2; 54/3		
54	X	29/4/5; 30/6/7/8		
55				
56	C1	55/1; 56/2/3		
57	C4	56/1; 58/3		
58	SUB	59/6		25V8
59	C2	59/1/3		
60	0V	60/1-12	11,12V2; 5,6V3;	1V8
61	$+U_p$	61/1-12	13V2;	21V7
62	$-U_N$	62/1-12	14,15V2; 29V6;	20V7

Note - The original signals above are incorrect, correct signals are shown to the right.

Board 5

Number	Signal name	Addresses of the field joints		
1	AU	2/4; 16/12		
2	MDS	2/2; 1/6		21V8
3	$\overline{S1}$	2/8		
4	F1	4/6/7; 5/8; 4/9; 5/10		3V7
5	SCHRF	5/9		
6	MV2			27V7
7	VLS	7/3/4; 6/8/9/10		
8	F3	8/3/6/7/8/9		5V7
9	M	9/9		6V8

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Fig. 38. Functional diagram of board 5.

Number	Signal name	Addresses of the field joints		
10	$\overline{\text{ST}}$	9/2; 10/6/7/8; 13/9		
11	MUL	9/3; 10/4; 11/6/7/8/9/10		17V8
12	$\overline{\text{F5}}$	27/2; 11/3; 12/6/7		
13	Z4	12/2/10; 11/11		11V7
14	U	13/4/6/7/8		
15	F5	11/2; 12/4; 15/6/7; 14/9		7V7
16	LES	15/2/4; 16/6		
17	X	17/4; 16/8/9; 13/10		
18	F2	17/6; 18/7; 17/8/9		4V7
19	S	20/4; 19/6; 20/7; 19/8; 20/9		
20	K66	19/4		
21	MV1			26V7
22	$\overline{Z}$	22/4/7; 21/8; 22/9; 20/10		
23	Z8	18/2; 23/7; 21/10; 23/11		12V7
24	DIV	24/6/7/8/9/10		
25	SCHREIB	24/1/2; 25/6/7		
26	$\overline{\text{VER}}$	24/3; 26/6/7/8/9/10		
27	$\overline{R}$	28/4/7; 27/8; 28/9/10		
28	S16	29/6/7; 28/8; 28/9/10		
29	$\overline{X}$	29/4; 30/6/7/8; 54/4		
30	AC	31/2/6		30V8
31	Z16	31/8/10		13V7
32	AC0	32/2/6		31V8
33	MRS	33/2/6		11V8
35	S1	36/2/4; 35/7; 34/8/10		7V8
36	V	37/3; 35/6		15V8
38	RÜ	37/6; 38/7; 39/8/9; 38/10	27V8	
39				
40	VER	40/3; 41/4; 39/6; 40/8; 41/9		28V8
41	$\overline{t}$	42/2		
43	$\overline{\text{Rü}}$	41/10		
44	$\overline{\text{F3}}$	42/6; 43/8		
46	K91	45/3		
48	K73	46/9		
51	HV	51/1		20V8
52	F6	51/6; 53/7; 52/9; 50/10		8V7
55	Z1	54/2; 48/10/11		9V7
59	Z2	57/2; 54/10; 52/11		10V7
60	0V	60/1-12	11,12V2; 5,6V3;	1V8
61	$+U_p$	61/1-12	13V2;	21V7
62	$-U_N$	62/1-12	14,15V2; 29V6;	20V7

Board 6

Number	Signal name	Addresses of the field joints		
1	MDS	2/2; 2/5		21V8
2	ADD1	3/4		
3	ADD	4/4; 3/8/9/10		
4	F1	4/5/7; 5/8; 4/9; 5/10		3V7
5	EING2	5/7		
7	R	8/4; 7/7/8/9/10		19V8
8	F3	8/3/5/7/8/9		5V7
10	$\overline{ST}$	9/2; 10/5/7/8; 13/9		
11	MUL	9/3; 10/4; 11/5/7/8/9/10		17V8
12	$\overline{F5}$	27/2; 11/3; 12/5/9		
13	U	13/4; 14/5; 13/7/8		
14	$\overline{F4}$	13/2; 14/3; 15/9		
15	F5	11/2; 12/4; 15/5/7; 14/9		7V7
16	LES	15/2/4; 16/5		
17	F2	18/5/7; 17/8/9		
18	F4	14/2; 19/7; 18/9		
19	S	20/4; 19/5; 20/7; 19/8; 20/9		
20	K112	20/3		
22	SvM	22/3		
24	DIV	24/5/7/8/9/10		18V8
25	SCHR	24/1/2; 25/5		5V8
26	$\overline{VER}$	24/3; 26/4/5/6/7/8/9/10		
27	$\overline{B4}$	27/3/7/9/10		18V7
29	S16	28/5; 29/7; 28/8; 29/9/10		
30	$\overline{X}$	29/54/4; 30/7/8; 29/5		
31	AC	31/2; 30/5		30V8
32	AC0	32/2/5		31V8
33	MRS	33/2/5		11V8
35	V	37/3; 36/5		15V8
36	B1	37/7		
37	Rü	38/5/7; 39/8/9; 38/10		27V8
39	VER	40/3; 41/4; 40/5/8; 41/9		28V8
41	A2F	42/3; 43/4		
42	$\overline{F3}$	44/5; 43/8		
43	$\overline{F2}$	43/3; 44/9; 43/10		
45	$\overline{S16}$	45/10		
51	F6	52/5; 53/7; 52/9; 50/10		8V7
52	$\overline{F1}$	50/8; 51/10		
54	K111	53/8		
55	$\overline{F6}$	53/3; 56/7; 54/8; 53/9		
57	$\overline{B1}$	57/3/7		15V7
59	SUB	58/4		25V8
60	0V	60/1-12	11,12V2; 5,6V3;	1V8
61	+U$_p$	61/1-12	13V2;	21V7
62	-U$_N$	62/1-12	14,15V2; 29V6;	20V7
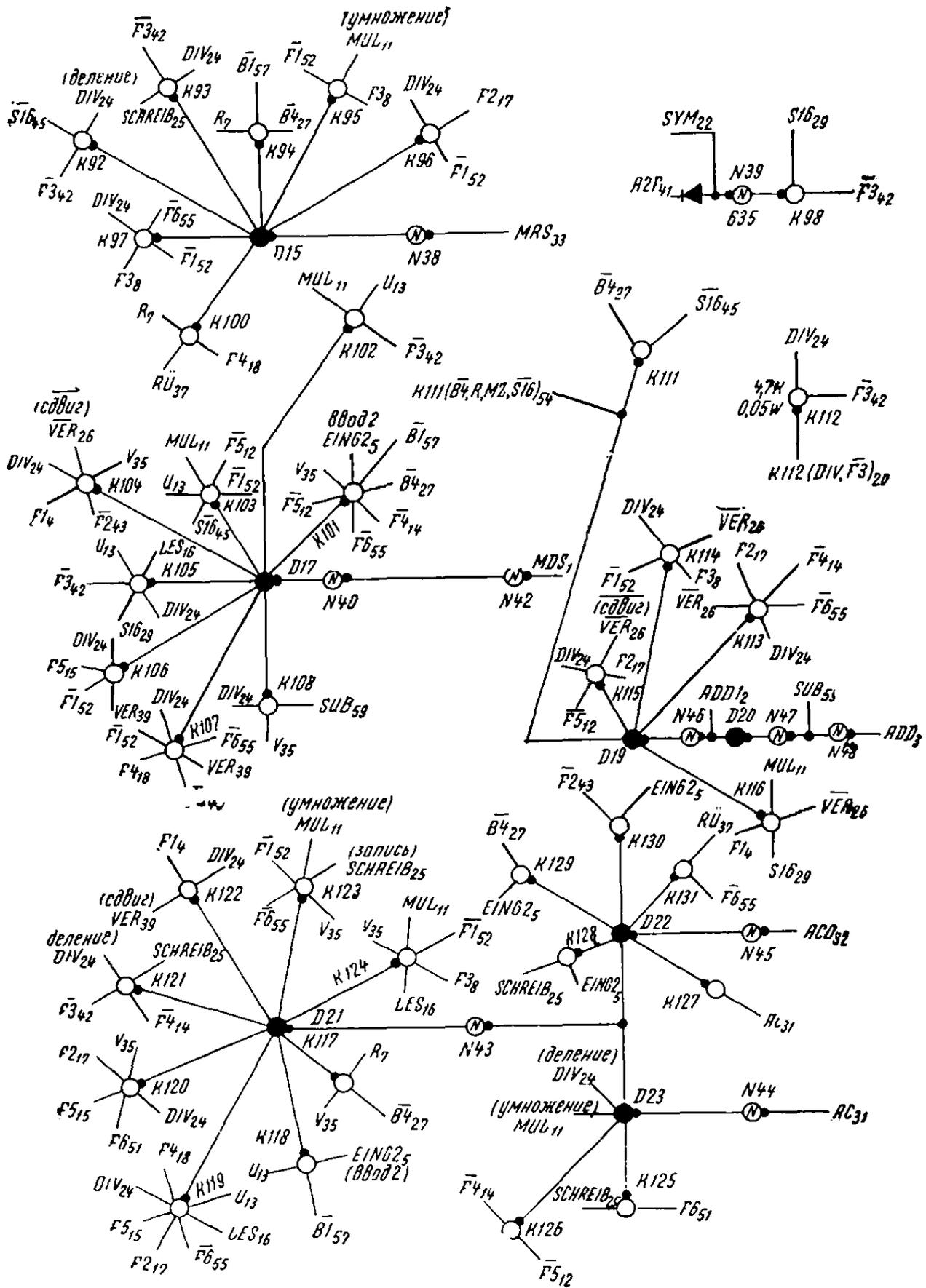
Fig. 39. Functional diagram of board 6.

Board 7

Number	Signal name	Addresses of the field joints	
1	ADD0	1/11	
2	K65	1/4/8	
4	F1	4/5/6; 5/8; 4/9; 5/10	
5	EiNG2	5/6	
6	$\overline{B3}$	4/3	
7	R	8/4; 7/6/8/9/10	19V8
8	F3	8/3/5/6/8/9	5V7
9	$\overline{KO}$	44/8; 45/9	
10	$\overline{ST}$	9/2; 10/5/6/8; 13/9	
11	MUL	9/3; 10/4; 11/5/6/8/9/10	17V8
13	U	13/4; 14/5; 13/6/8	
15	F5	11/2; 12/4; 15/5/6; 14/9	7V7
18	F2	18/5; 17/6/8/9	4V7
19	F4	14/2; 18/6/9	6V7
20	S	20/4; 19/5/6/8; 20/9	
21	EiNG	21/4; 22/8; 19/9; 43/9; 42/8	
22	$\overline{Z}$	22/4/5; 21/8; 22/9; 20/10	
23	Z8	18/2; 23/5; 21/10; 23/11	12V7
24	DIV	24/5/6/8/9/10	18V8
25	$\overline{MUL}$	25/4/9/10	
26	$\overline{VER}$	24/3; 26/4/5/6/8/9/10	
27	$\overline{B4}$	27/3/6/9/10	18V7
28	$\overline{R}$	28/4; 27/5/8; 28/9/10	
29	$\overline{S16}$	28/5; 29/6; 28/8; 29/9/10	
30	$\overline{X}$	29,54/4; 30/6/8; 29/5	
31	K182	30/10	
32	:0	32/11	
33	Z+E8	33/4/8/9; 32/10	
34	G2	34/4; 33/10	
35	S1	3/2/4; 35/5; 34/8/10	7V8
36	K140	36/8	
37	BI	36/6	
38	Ru	38/5; 37/6; 39/8/9; 38/10	27V8
40	VOR		
41	A8F	41/3; 42/4	
42	(=)0	43/11	
44	B2		16V7
45	(X)0	45/11	
46	B3		17V7
47	$\overline{VOR}$	47/8	29V8
48	B4		
49	$\overline{B2}$	49/3	
51	K132	50/3	
52	Lo	51/8; 50/9	31V4
53	F6	52/5; 51/6; 52/9; 50/10	8V7
55	ST+KO	53/10	
56	$\overline{F6}$	53/3; 55/6; 54/8; 53/9	

Fig. 40. Functional diagram of board 7.

Number	Signal name	Addresses of the field joints		
57	$\overline{B1}$	57/3/6	15V7	
58	K194	59/10		
59	FU0	59/9/11		
60	0V	60/1-12	11,12V2; 5,6V3;	1V8
61	$+U_P$	61/1-12	13V2;	21V7
62	$-U_N$	62/1-12	14,15V2; 29V6;	20V7

Board 8

Number	Signal name	Addresses of the field joints
1	K65	1/4, 2/7
2	$\overline{S1}$	3/5
3	ADD	4/4, 3/6/9/10
4	K155	4/10
5	F1	4/5/6/7/9; 5/10
6	VLS	7/3/4/5; 6/9/10
7	R	8/4; 7/6/7/9/10
8	F3	8/3/5/6/7/9
9	$\overline{MZ}$	9/4; 10/9
10	$\overline{ST}$	9/2; 10/5/6/7; 13/9
11	MUL	9/3; 10/4; 11/5/6/7/9/10
12	LMZ	
13	U	13/4; 14/5; 13/6/7
15	K186	14/10
16	X	17/4/5; 16/9; 13/10
17	F2	18/5; 17/6; 18/7; 17/9
18	SuBO	18/11
19	S	20/4; 19/5/6; 20/7/9
20	A1	15/1; 16/3/4; 19/10
21	$\overline{Z}$	22/45/7/9; 20/10
22	EING	21/4/7; 19/9; 42/8; 43/9
23	K144	23/9
24	DIV	24/5/6/7/9/10
26	$\overline{VER}$	24/3; 26/4/5/6/7/9/10
27	$\overline{R}$	28/4; 27/5; 28/7/9/10
28	S16	28/5; 29/6/7/9/10
29	MZ	28/3
30	$\overline{X}$	29/54/4; 30/6/7; 29/5
31	Z16	31/5/10
32	$\overline{ÜBER}$	32/4/9
33	Z+E8	33/4/7/9; 32/10
34	S1	36/2/4; 35/5/7; 34/10
35	K183	35/10
36	K140	36/7

Fig. 41. Functional diagram of board 8.

Number	Signal name	Addresses of the field joints		
39	Rü	38/5; 37/7; 38/; 39/9; 38/10;		27V8
40	VER	40/3; 41/4; 40/5; 39/6; 41/9;		28V8
42	EING	21/4/7; 22/8; 19,43/9		
43	$\overline{F3}$	44/5; 42/6		
44	$\overline{K0}$	45/9; 9/7		
45	A4	44/1/3/4		22V8
46	UBER	47/4/9; 46/10		2V7
47	$\overline{VOR}$	47/7		29V8
48	K152	46/3		
49	Z10	48/9; 49/12		
50	$\overline{F1}$	52/6; 51/10		
51	Lo	52/7; 50/9		31V4
52	G1	52/3/4/10		
53	K111	54/6		
54	$\overline{F6}$	53/3; 55/6; 56/7; 53/9		
55	K153	54/9		
56	CO	57/12		
57	K160	57/9/10		
60	0V	60/1-12	11,12V2; 5,6V3;	1V8
61	$+U_p$	61/1-12	13V2;	21V7
62	$-U_N$	62/1-12	14,15V2; 29V6;	20V7

Board 9

Number	Signal name	Addresses of the field joints	
1	K162	1/2	
2	(±)0	3/11	
3	ADD	4/4; 3/6/8/10	
4	F1	4/5/6/7; 5/8/10	3V7
5	SCHRF	5/5	
6	VLS	7/3/4/5; 6/8/10	
7	R	8/4; 7/6/7/8/10	19V8
8	F3	8/3/5/6/7/8	5V7
9	M	9/5	6V8
10	$\overline{MZ}$	9/4/8	26V8
11	MUL	9/3; 10/4; 11/5/6/7/8/10	17V8
12	$\overline{F5}$	27/2; 11/3; 12/5/6	
13	$\overline{ST}$	9/2; 10/5/6/7/8	
14	F5	11/2; 12/4; 15/5/6/7	7V7
15	$\overline{F4}$	13/2; 14/3/6	
16	X	17/4/5; 16/8; 13/10	
17	F2	18/5; 17/6; 18/7; 17/8	4V7
18	F4	14/2; 18/6; 19/7	6V7
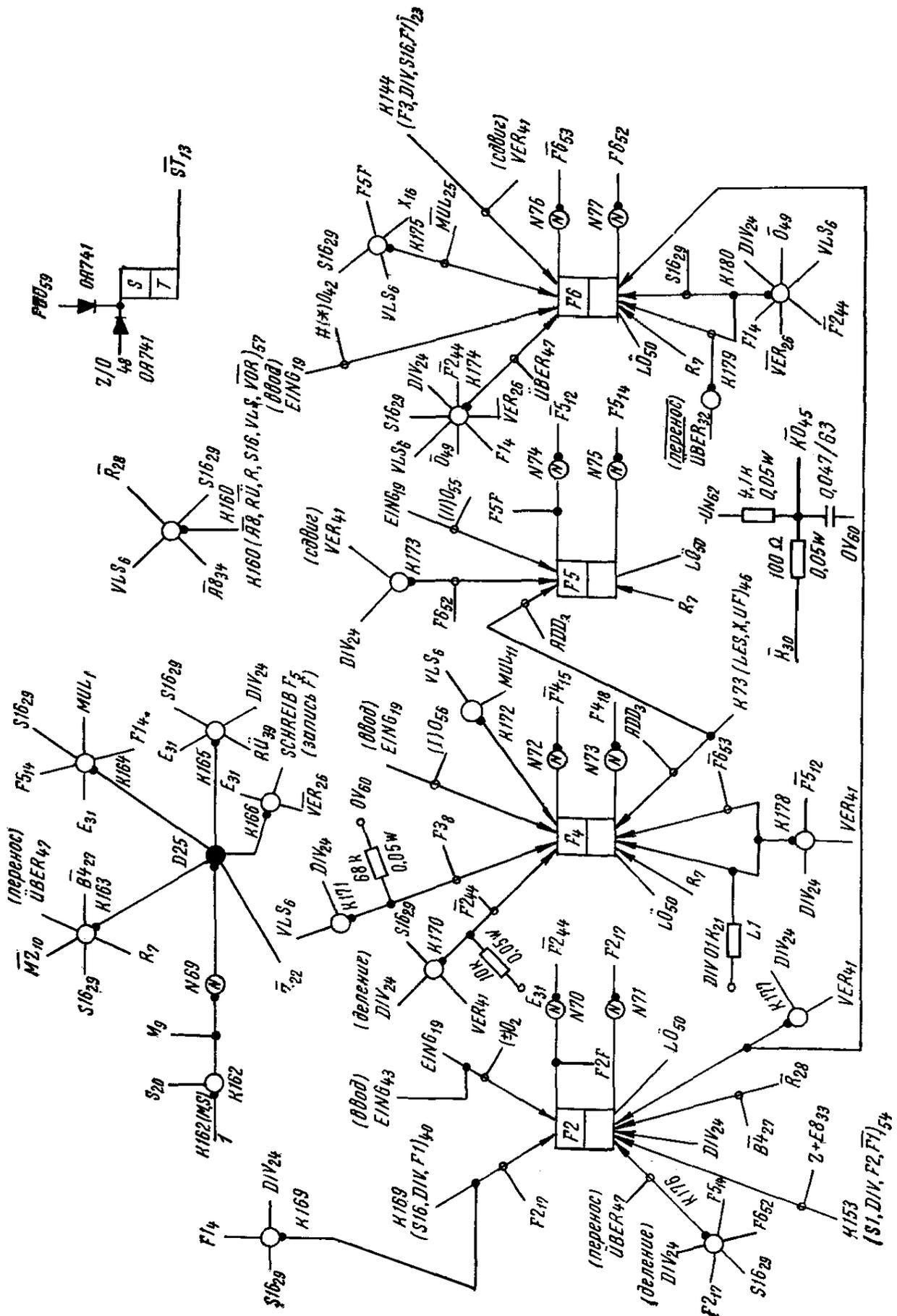
Fig. 42. Functional diagram of board 9.

Fig. 43. Functional diagram of board 10.

Number	Signal name	Addresses of the field joints		
19	EING	21/4/7; 22/8; 42/8; 43/9		
20	S	20/4; 19/5/6; 20/7; 19/8		
21	DIV 01k			9V5
22	$\overline{Z}$	22/4/5/7; 21/8; 20/10		
23	K144	23/8		
24	DIV	24/5/6/7/8/10		18V8
25	$\overline{MUL}$	25/4/7/10		
26	$\overline{VER}$	24/3; 26/4/5/6/7/8/10		
27	$\overline{B4}$	27/3/6/7/10		18V7
28	$\overline{R}$	28/4; 27/5; 28/7; 27/8; 28/10		
29	S16	28/5; 29/6/7; 28/8; 29/10		
30	$\overline{K}$			7V3
31	E	31/4		
32	$\overline{UBER}$	32/4/8		
33	Z+E8	33/4/7/8; 32/10		
34	$\overline{A8}$	48/1/3		
39	Rü	38/5; 37/6; 38/7; 39/8; 38/10		27V8
40	K169	40/10		
41	VER	40/3; 41/4; 40/5; 39/6; 40/8;		28V8
42	#(*)0	44/11		
43	EING	21/4/7; 22,42/8; 19/9		
44	$\overline{F2}$	43/3/6/10		
45	$\overline{KO}$	44/8; 9/7		
46	K73	48/5		
47	UBER	47/4; 46/8/10		2V7
48	Z/0	49/8/12		
49	$\overline{O}$	48/4; 40/12		
50	Lö	52/7; 51/8		31V4
52	F6	52/5; 51/6; 53/7; 50/10		8V7
53	$\overline{F6}$	53/3; 55/6; 56/7; 54/8		
54	K153	55/8		
55	(II)0	53/11		
56	(I)0	54/11		
57	K160	57/8/10		
59	Fu0	59/7/10		
60	0V	60/1-12	11,12V2; 5,6V3;	1V8
61	$+U_p$	61/1-12	13V2;	21V7
62	$-U_N$	62/1-12	14,15V2; 29V6;	20V7

Board 10

Number	Signal name	Addresses of the field joints	
1	G24		6V5
2	G28		7V5
3	ADD	4/4; 3/6/8/9	

Number	Signal name	Addresses of the field joints		
4	K155	4/8		
5	F1	4/5/6/7; 5/8; 4/9		3V7
6	VLS	7/3/4/5; 6/8/9		
7	R	8/4; 7/6/7/8/9		19V8
8	G22			5V5
10	G11			1V5
11	MUL	9/3; 10/4; 11/5/6/7/8/9		17V8
12	Z4	12/2; 13/5; 11/11		11V7
13	X	17/4/5; 16/8/9		
14	K186	15/8		
18	G18			3V5
19	A1	15/1; 16/3/4; 20/8		2V8
20	$\overline{Z}$	22/4/5/7; 21/8; 22/9		
21	Z8	18/2; 23/5/7/11		12V7
22	$\overline{Z8}$	29/2; 28/11		
23	$\overline{Z4}$	30/2; 29/11		
24	$\overline{DIV}$	24/5/6/7/8/9		18V8
25	$\overline{MUL}$	25/4/7/9		
26	$\overline{VER}$	24/3; 26/4/5/6/7/8/9		
27	$\overline{B4}$	27/3/6/7/9		18V7
28	$\overline{R}$	28/4; 27/5; 28/7; 27/8; 28/9		
29	S16	28/5; 29/6/7; 28/8; 29/9		
30	K182	31/7		
31	Z16	31/5/6		
32	Z+E8	33/4/7/8/9		
33	G2	34/4/7		
34	S1	36/2/4; 35/5/7; 34/8		7V8
35	K183	35/8		
38	RÜ	38/5; 37/6; 38/7; 39/8/9		27V8
39	G14			
40	K169	40/9		
41	$\overline{Ru}$	43/5		
43	$\overline{F2}$	43/3/6; 44/9		
45	$\overline{S16}$	45/6		
46	UBER	47/4; 46/8; 47/9		2V7
47	G21			
48	Z1	54/2; 55/5; 48/11		9V7
49	$\overline{Z1}$	58/2; 49/11		
50	F6	52/5; 51/6; 53/7; 52/9		8V7
51	$\overline{F1}$	52/6; 50/8		
52	G1	52/3/4/8		
53	ST+KO	55/7		
54	Z2	57/2; 59/5; 52/11		10V7
55	$\overline{Z2}$	59/2; 51/11		
57	K160	57/8/9		
59	K194	58/7		
60	0V	60/1-12	11,12V2; 5,6V3;	1V8
61	$+U_p$	61/1-12	13V2;	21V7
62	$-U_N$	62/1-12	14,15V2; 29V6;	20V7

Board 11

Number	Signal name	Addresses of the field joints	
1	ADD0	1/7	
2	UA0	4/12	8V2
3	(±)0	2/9	
4	SV1		12V6
5	SV2		13V6
6	SV3		14V6
7	SV4		15V6
8	SV5		16V6
9	SV6		17V6
10	SV7		18V6
11	Z4	12/2; 13/5; 12/10	11V7
12	SV8		19V6
13	SV9		20V6
14	$+U_{A1}$		24V7
15	SV10		21V6
16	SV11		22V6
17	+ IIк		20V4
18	SUBO	18/8	
19	+ IIIк		21V4
21	-K		13V4
22	+K		12V4
23	Z8	18/2; 23/5/7; 21/10	12V7
24	#K		20V3
25	+ IIIк		27V4
26	- IIIк		24V4
27	+ IK		19V4
28	$\overline{Z8}$	29/2; 22/10	
29	$\overline{Z4}$	30/2; 23/10	
30	1K		15V4
31	▼IIIк		30V4
32	:0	32/7	
33	- Iк		22V4
34	- IIк		23V4
35	X^Nк		16V4
36	▼Iк		28V4
37	* IIк		26V4
38	* IIк		25V4
40	▼IIк		29V4
41	Xк		14V4
42	=к		17V4
43	(=)0	42/7	
44	#(*)0	42/9	
45	(X)0	45/7	
48	Z1	54/2; 55/5; 48/10	9V7
49	$\overline{Z1}$	58/2; 49/10	
51	$\overline{Z2}$	59/2; 55/10	
52	Z2	57/2; 59/5; 54/10	10V7
53	(II)0	55/9	
54	(I)0	56/9	
55	SV12		23V6

Fig. 44. Functional diagram of board 11.

Number	Signal name	Addresses of the field joints		
56	SV13			24V6
57	SV14			25V6
58	SV15			26V6
59	FU0	59/7/9		
60	0V	60/1-12	11,12V2; 5,6V3;	1V8
61	$+U_p$	61/1-12	13V2;	21V7
62	$-U_N$	62/1-12	14,15V2; 29V6;	20V7

Board 12

Number	Signal name	Addresses of the field joints	
1	7	1/3	
2	8	2/3	
4	UAO	2/11	8V2
5	3	2/1	
6	9	5/3/4	
7	ZV7		7V6
8	ZV3		3V6
9	ZV9		9V6
11	$-U_A$		7V2
15	ZV8		8V6
16	AU	2/4; 1/5	
17	ZV6		6V6
20	ZV4		
22	Z/20	11/4	
24	ZV5		
28	4	28/1	
29	2	30/1	
30	5	30/3	
31	6	31/3	
32	ZV2		2V6
34	Z/80	38/4	
35	Z/40	37/4	
36	ZV0		10V6
38	ZV1		1V6
40	$\overline{0}$	48/4; 49/8	
41	1	40/4	
42	Z/10	50/4	
43	,к		11V4
44	Cк		18V4
45	9к		9V4
46	8к		8V4
47	7к		7V4
48	6к		6V4

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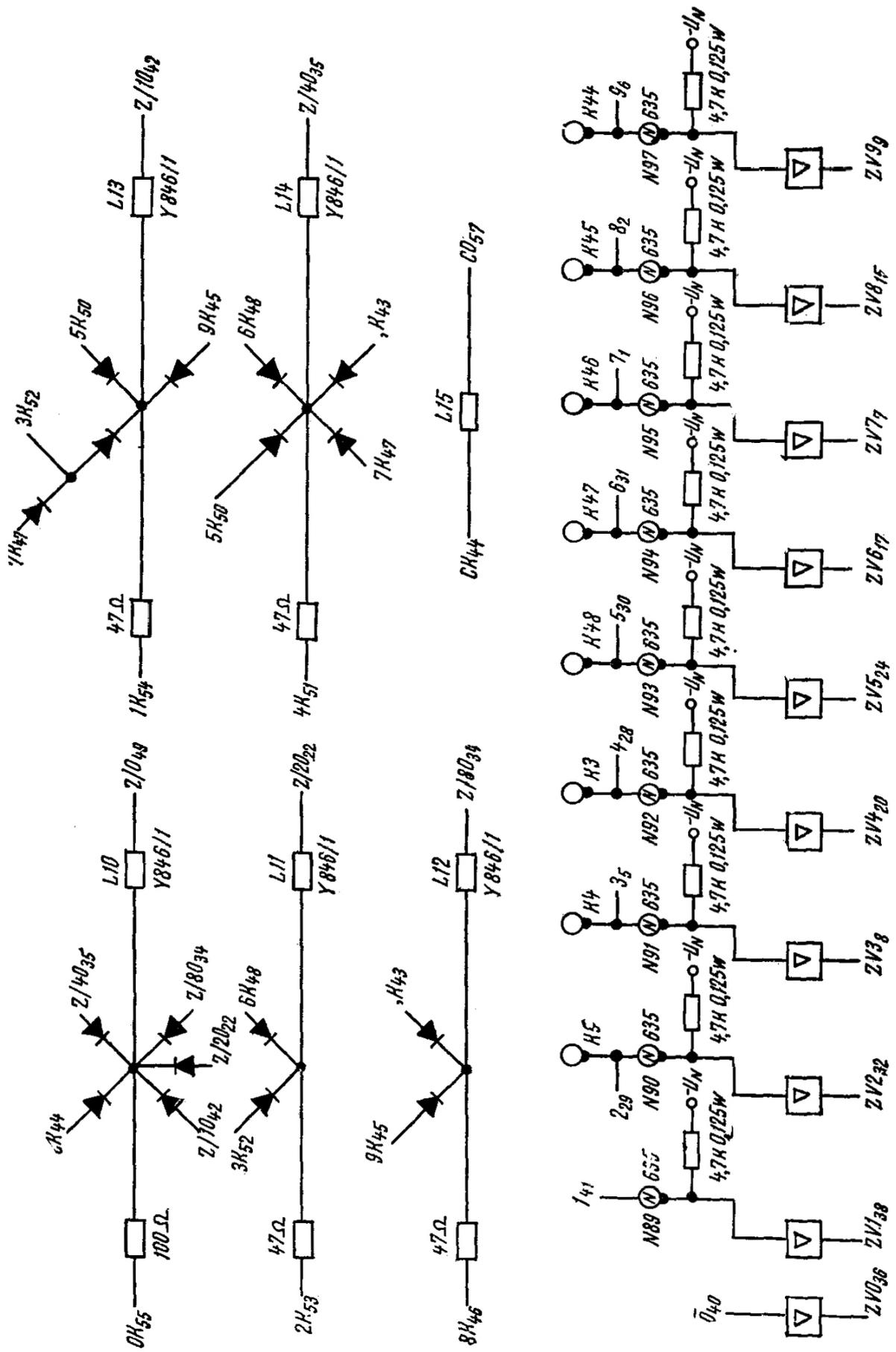
Fig. 45. Functional diagram of board 12.

Number	Signal name	Addresses of the field joints		
49	Z/0	49/8; 48/9		
50	5 к	5V4		
51	4 к	4V4		
52	3 к	3V4		
53	2 к	2V4		
54	1 к	1V4		
55	0 к	10V4		
56	CO	56/8		
57	0V	60/1 – 12	11, 12V2; 5, 6V3;	1V8
60	$+U_P$	61/1 – 12	13V2;	21V7
61	$-U_N$	62/1 – 12	14, 15V2; 29V6;	20V7

IV. 3. DETERMINATION OF RESISTOR VALUES

The coloured rings, indicated by paint on the surface of a resistor with reference to one of the examples, determine the resistance of the resistor in the ohms. A reading is taken from the track nearest to the resistor end, which is counted first .

The first ring colour determines the first number; the colour of the second ring - the second number; and the colour of the third ring determines the quantity of zeros after the second number.

For example:
1st - Red;   2nd - Green;   3rd - Yellow,   I.E. 250000 ohms;
1st - Blue; 2nd - Red;   3rd - Brown,   I.E. 620 ohms.
     6   2   0

The fourth ring determines permissible percentage deviation in the value of the resistor.

Gold colour of ring - ± 5%; silver - ± 10%. The absence of the fourth ring corresponds to a permissible deviation of ± 20%.

Table 1
Determination of resistor value
from the ring colour.

Ring colour	Ring		
	1	2	3
Black	-	0	0
Brown	1	1	1
Red	2	2	2
Orange	3	3	3
Yellow	4	4	4
Green	5	5	5
Blue	6	6	6
Violet	7	7	7
Grey	8	8	8
White	9	9	9

Table 2
Determination of the resistor
power and overall sizes

Resistor power (W)	Diameter (mm)	Length (mm)
0,05	2,3	6,5
0,125	2,3	11,5
0,25	5	17
0,5	5	26
1	8	32
2	9	55

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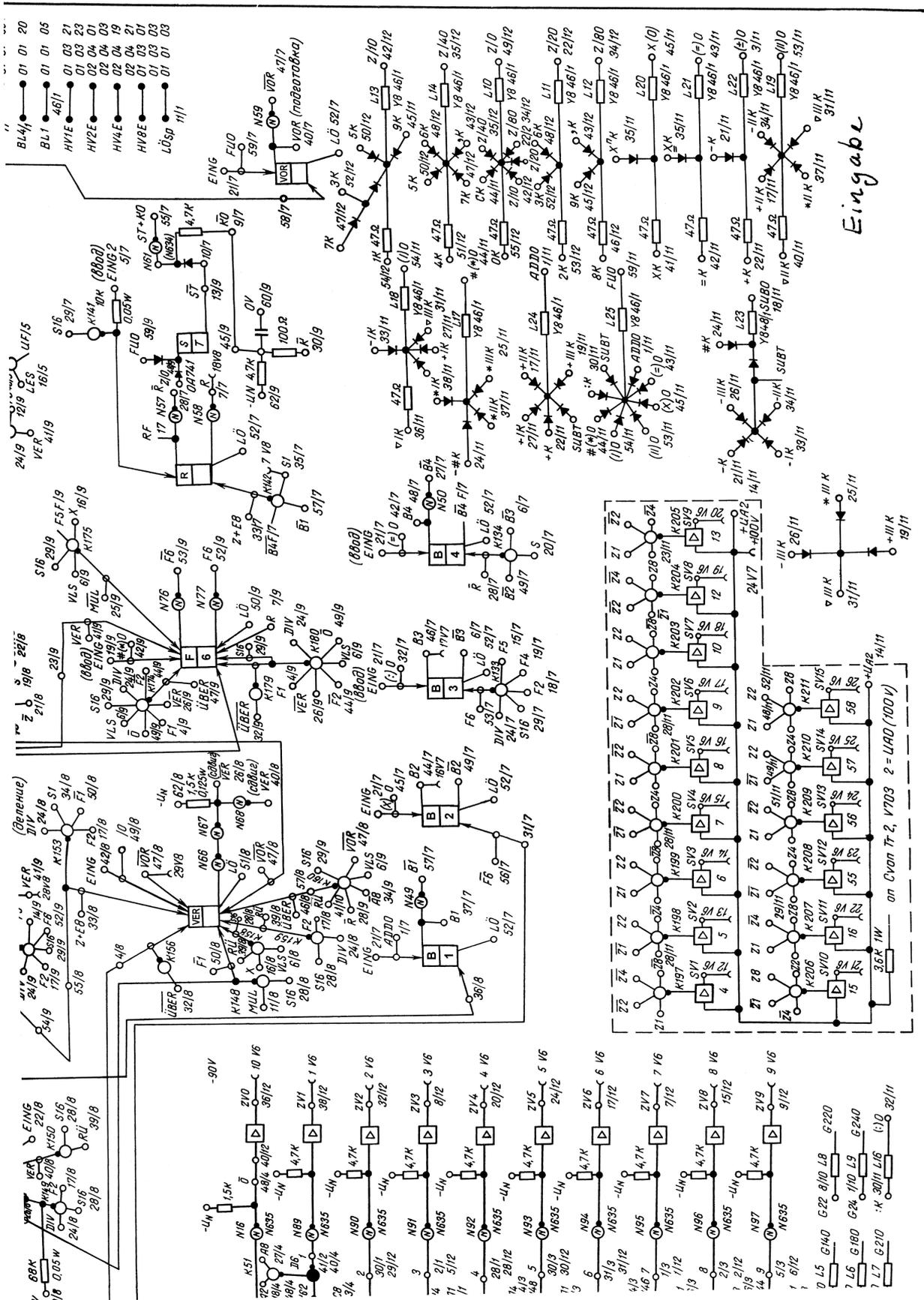
Alexander Gavrilovic Bobrov
Ivan Iosifovich Bigler

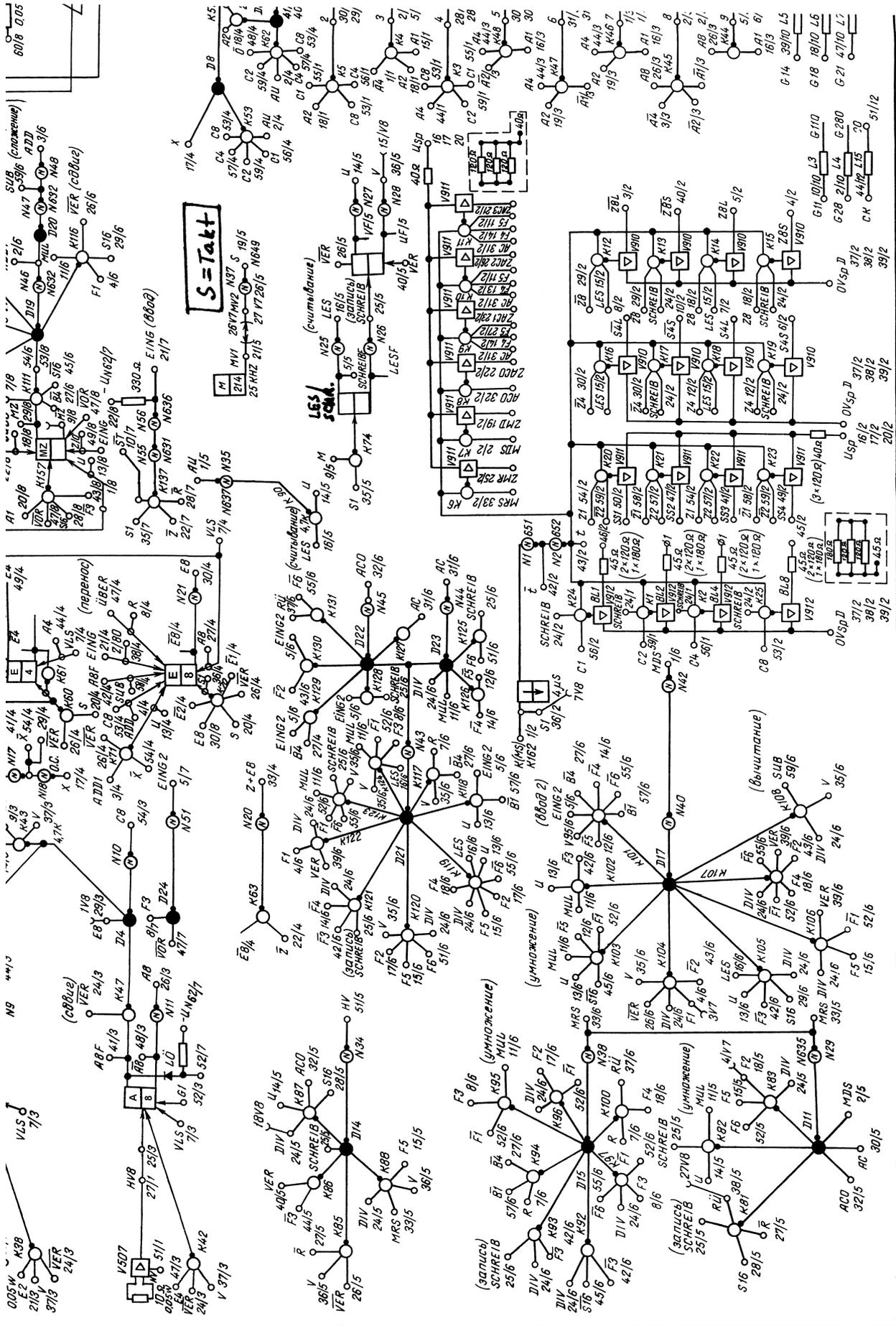**Design, Maintenance, Service and Operation EKVM**
"Soemtron-220"

(логическая) схема машины.

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Рис. 30. Общая функциональная (ло

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