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Entitled

ELEKTRONISCHER TISRECHNER Technische Instruktion Teil II

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It has been published by us to disseminate information about the Soemtron 22x range of electronic desk calculators manufactured by V.E.B. (*1) Büromaschinenwerk Sömmerda, as a project to gather and centralise whatever information can be found about these increasingly rare early electronic calculators.

If you have or know of any information, books, drawings, circuits, hardware, test equipment (**Prüfgerät**) or other memorabilia relating to the Soemtron 220, 221, 222 or 224 calculators, their trade names - Daro or Soemtron, manufactured by - V.E.B. Büromaschinenwerk Sömmerda, please email us at - mike@soemtron.org

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With this effort in mind some of the syntax presented here is a little strange to say the least!. Some portions have been reworked to be more readable English text but there is obviously more to be done. If you can help with this, or indeed have any helpful information or comments, please email us at - mike@soemtron.org

Please use, and hopefully enjoy, this information in the spirit in which we undertook to generate it - as an information source for an interesting piece of early calculator history before the advent of modern electronics, in the days when “hands on” engineers thought through the problems and challenges of designing equipment with little resources, to produce the best end product they could.

June 2017

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*1 - V.E.B - Volkes Eigener Betrieb = Peoples Owned Company



ELECTRONIC DESK CALCULATOR

- Edition February 1974 -

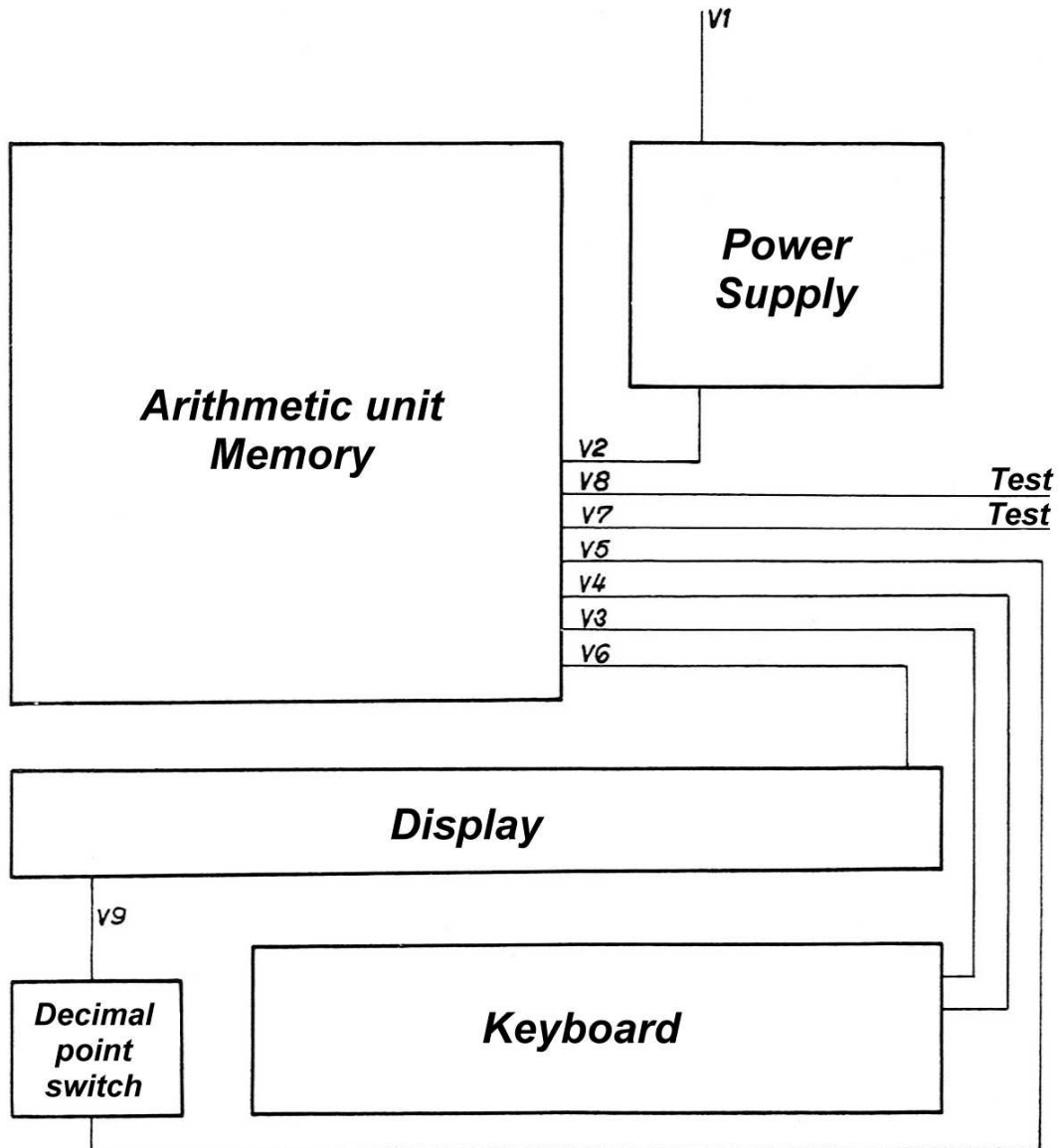
Technical Instruction
Part ii

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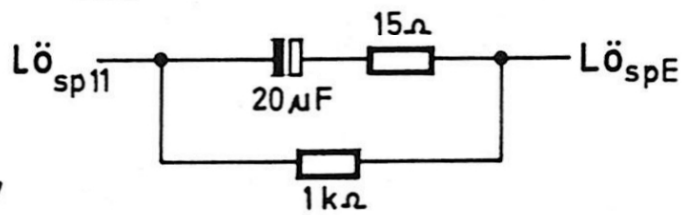
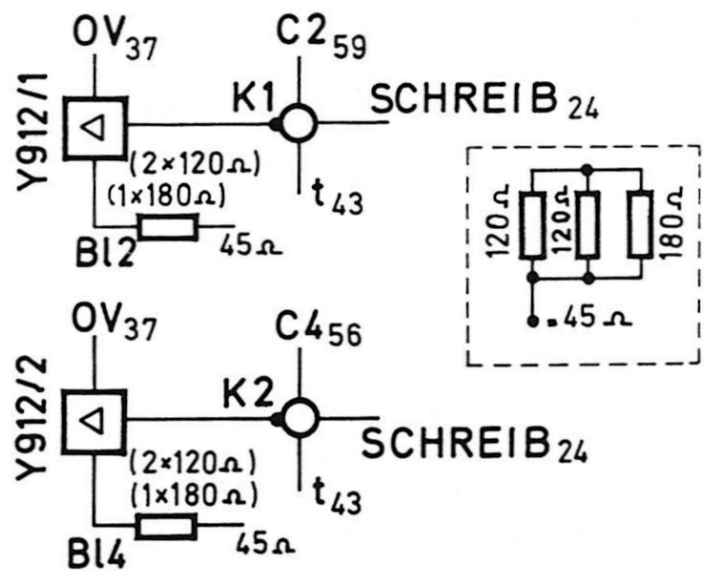
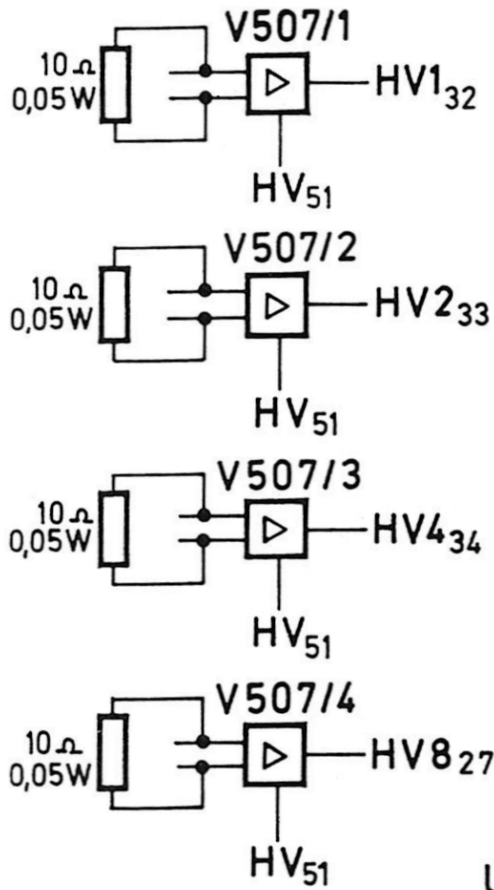
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Block diagram with connector numbers



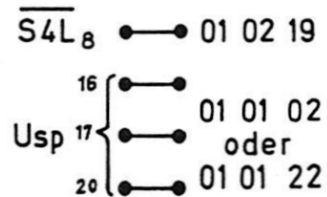
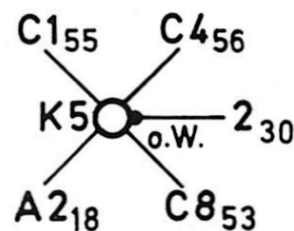
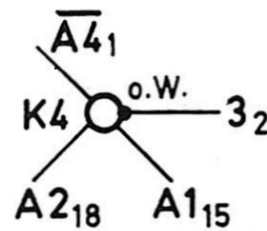
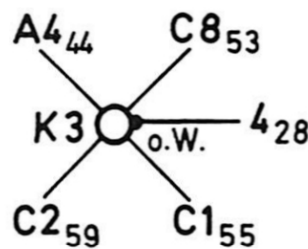
1	A4	3/3	
2	3	5/12	
3	Z8L	3/2	
4	Z8S	4/2	
5	Z8L	5/2	
6	S4S	6/2	
7	S4L	7/2	
8	Z4L	8/2	
9			
10	S4S	10/2	
11	Lösp		32V4
12	Al		
13			
14	Al		
15	Al	16/3/4; 20/8; 19/10	2V8
16	-Usp	20/2	9,10V2
17	-Usp	20/2	9,10V2
18	A2	19/3; 18/4	12V8
19	ZMD	19/2	
20	-Usp	20/2	9,10V2
21	ZAC3	21/2	
22	ZACO	22/2	
23	ZAC1	23/2	
24	SCHR	24/2; 25/5/6	5V8
25	ZMR	25/2	
26	ZAC2	26/2	
27	HV8	25/3	
28	4	28/12	
29	HV8		
30	2	29/12	
31	HV8		
32	HV1		32/3
33	HV2	33/3	
34	HV4	34/3	
35			
36			
37	OVspA	37/2	17V3
38	OVspA	38/2	18V3
39	OVspA	39/2	19V3
40	Z8S	40/2	
41	SS3	41/2	
42			
43	t	43/2	
44	A4	44/3/4; 45/8	22V8
45	BL8	45/2	
46	BL1	46/2	
47	SS2	47/2	
48	A8	48/3;	34/9
49	SS4	49/2	
50	SS1	50/2	
51	HV	51/5	20V8
52	OVsp		
53	C8	53/2; 54/3; 53/4	
54	C4		
55	Cl	56/2/3/4	
56	C4	58/3;	57/4
57	C2		
58			
59	C2	59/3/4	
60	0V	60/1-12	11,12V2; 5,6V3; 1V8
61	+Up	61/1-12	13V2; 21V7
62	-Un	62/1-12	14,15V2; 29V6; 20V7

Pin assignment - Board 1



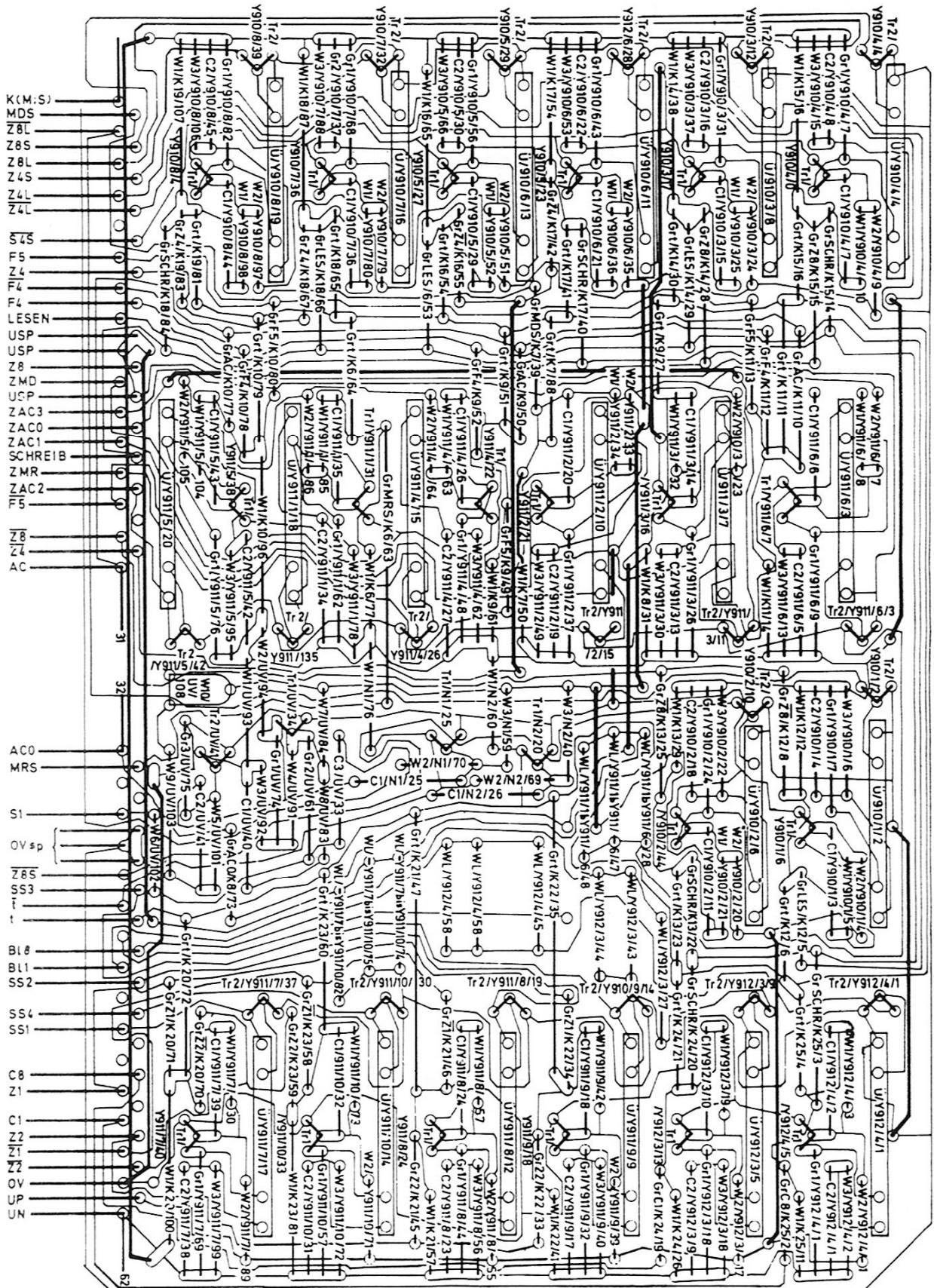
Anschlüsse für Speicher

- ZMR₂₅ ●—● 01 03 17
- ZMD₁₉ ●—● 01 01 10
- ZAC0₂₂ ●—● 01 03 13
- ZAC1₂₃ ●—● 01 01 14
- ZAC2₂₆ ●—● 01 03 09
- ZAC3₂₁ ●—● 01 01 18
- Z8S₄ ●—● 01 01 16
- Z8L₅ ●—● 01 03 19
- Z8S₄₀ ●—● 01 01 04
- Z8L₃ ●—● 01 03 07
- SS₄₄₉ ●—● 01 04 18
- SS1₅₀ ●—● 01 02 05
- SS2₄₇ ●—● 01 04 14
- SS3₄₁ ●—● 01 02 09
- S4S₆ ●—● 01 04 04
- S4L₇ ●—● 01 02 03
- S4S₁₀ ●—● 01 04 20



- S4L₈ ●—● 01 02 19
- Usp₁₆ ●—● 01 01 02
- Usp₁₇ ●—● 01 01 02
- Usp₂₀ ●—● 01 01 22
- Bl8₄₅ ●—● 01 01 19
- Bl2 ●—● 01 01 06
- Bl4 ●—● 01 01 20
- Bl1₄₆ ●—● 01 01 05
- HV1E ●—● 01 03 21
- HV2E ●—● 01 03 23
- HV4E ●—● 02 04 01
- HV4E ●—● 02 04 03
- HV4E ●—● 02 04 19
- HV8E ●—● 02 04 21
- HV8E ●—● 01 03 01
- HV8E ●—● 01 03 03
- LöspE ●—● 01 01 03

Logic diagram - Board 1

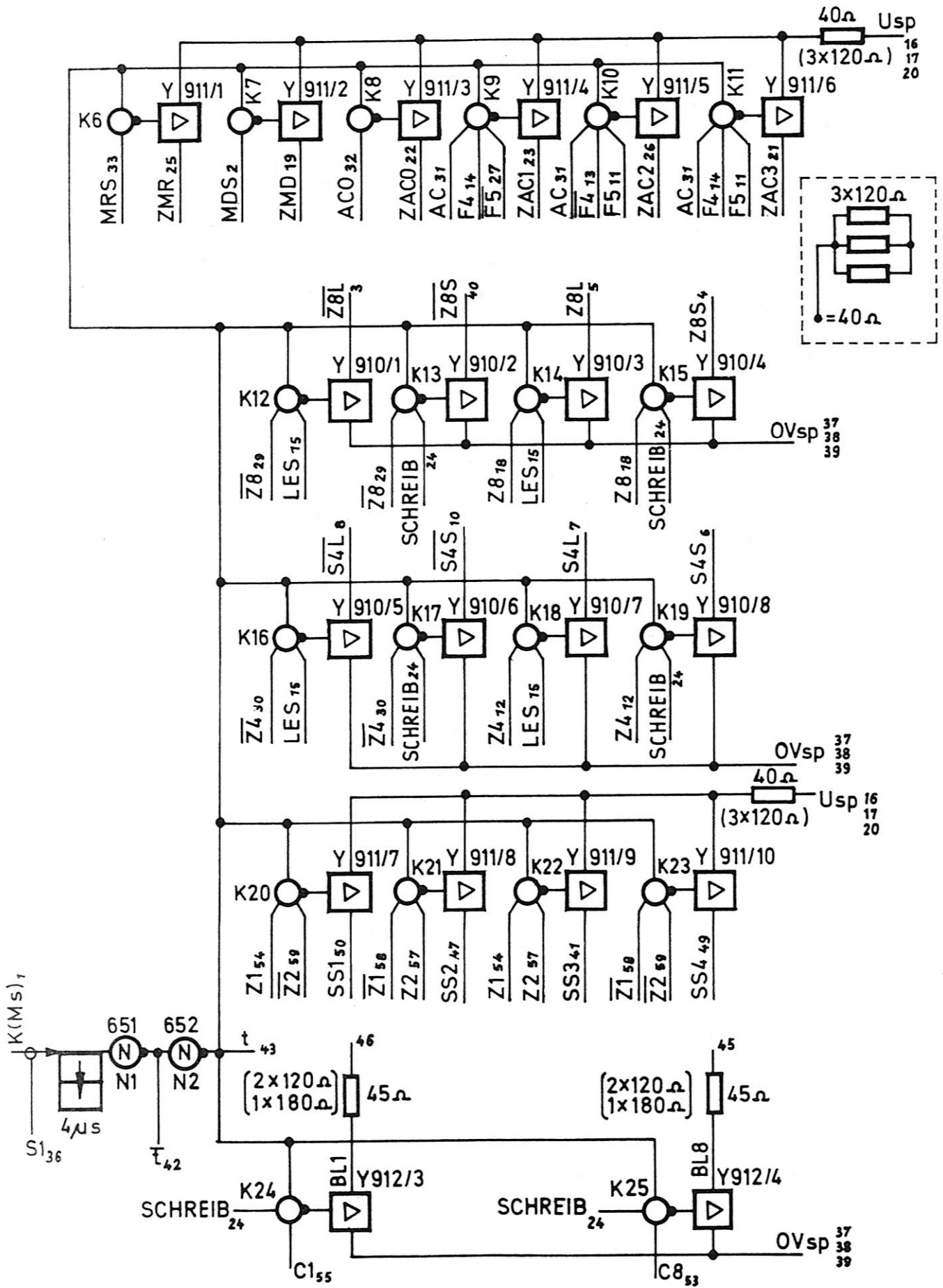


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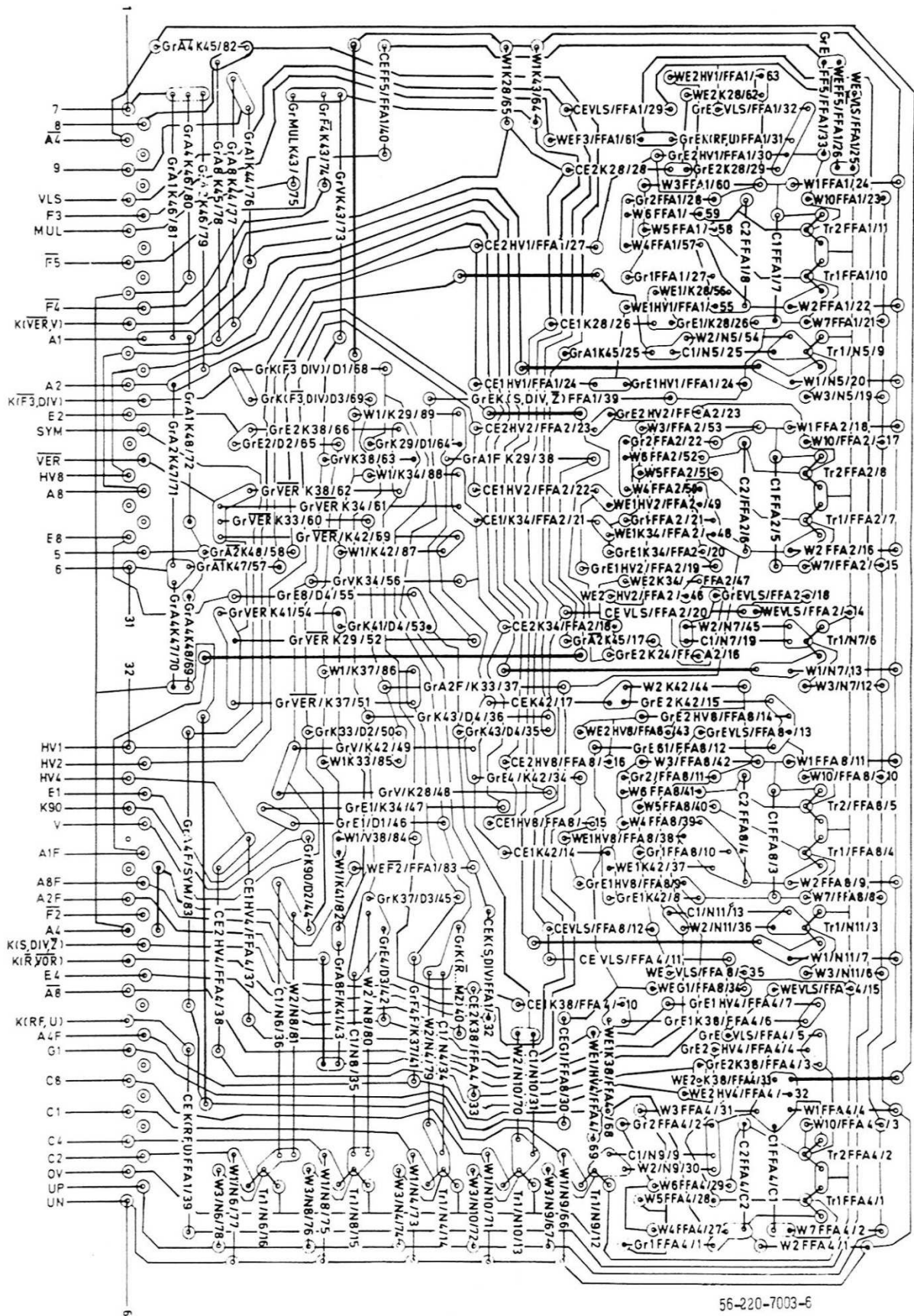
Layout plan - Board 2

1	K162	1/9	
2	MDS	2/5; 1/6	
3	<u>Z8L</u>	3/1	
4	Z8S	4/1	
5	Z8L	5/1	
6	S4S	6/1	
7	S4L	7/1	
8	<u>S4L</u>	8/1	
9	<u>ST</u>		10/5/6/7/8; 13/9
10	S4S	10/1	
11	F5	12/4; 15/5/6/7; 14/9	7V7
12	Z4	13/5; 12/10; 11/11	11V7
13	<u>F4</u>	14/3/6; 15/9	
14	F4	18/6; 19/7; 18/9	6V7
15	LES	15/4; 16/6/6	
16	-Usp	20/1	9,10V2
17	-Usp	20/1	9,10V2
18	Z8	23/5/7; 21/10; 23/11	12V7
19	ZMD	19/1	
20	-Usp	20/1	9,10V2
21	ZAC3	21/1	
22	ZACO	22/1	
23	ZAC1	23/1	
24	SCHR	24/1; 25/5/6	5V8
25	ZMR	25/1	
26	ZAC2	26/1	
27	<u>F5</u>	11/3; 12/5/6/9	
28			
29	<u>Z8</u>	22/10; 28/11	
30	<u>Z4</u>	23/10; 29/11	
31	AC	30/5; 31/6	30V8
32	ACO	32/5/6	31V8
33	MRS	33/5/6	11V8
34			
35			
36	S1	36/4; 35/5/7; 34/8/10	7V8
37	0Vsp	37/1	17V3
38	0Vsp	38/1	18V3
39	0Vsp	39/1	19V3
40	<u>Z8S</u>	40/1	
41	SS3	41/1	
42			
43	t	41/5	
44	t	43/1	
45	BL8		45/1
46	BL1	46/1	
47	SS2	47/1	
48			
49	SS4	49/1	
50	SS1	50/1	
51			
52			
53	C8	53/1; 54/3; 53/4	
54	Z1	55/5; 48/10/11	9V7
55			
56	Cl	55/1; 56/3/4	
57	Z2	59/5; 54/10; 52/11	10V7
58	<u>Z1</u>	49/10/11	
59	<u>Z2</u>	55/10; 51/11	
60	0V	60/1-12	11,12V2; 5,6V3; 1V8
61	+Up	61/1-12	13V2; 21V7
62	-Un	62/1-12	14,15V2; 29V6; 20V7

Pin assignment - Board 2



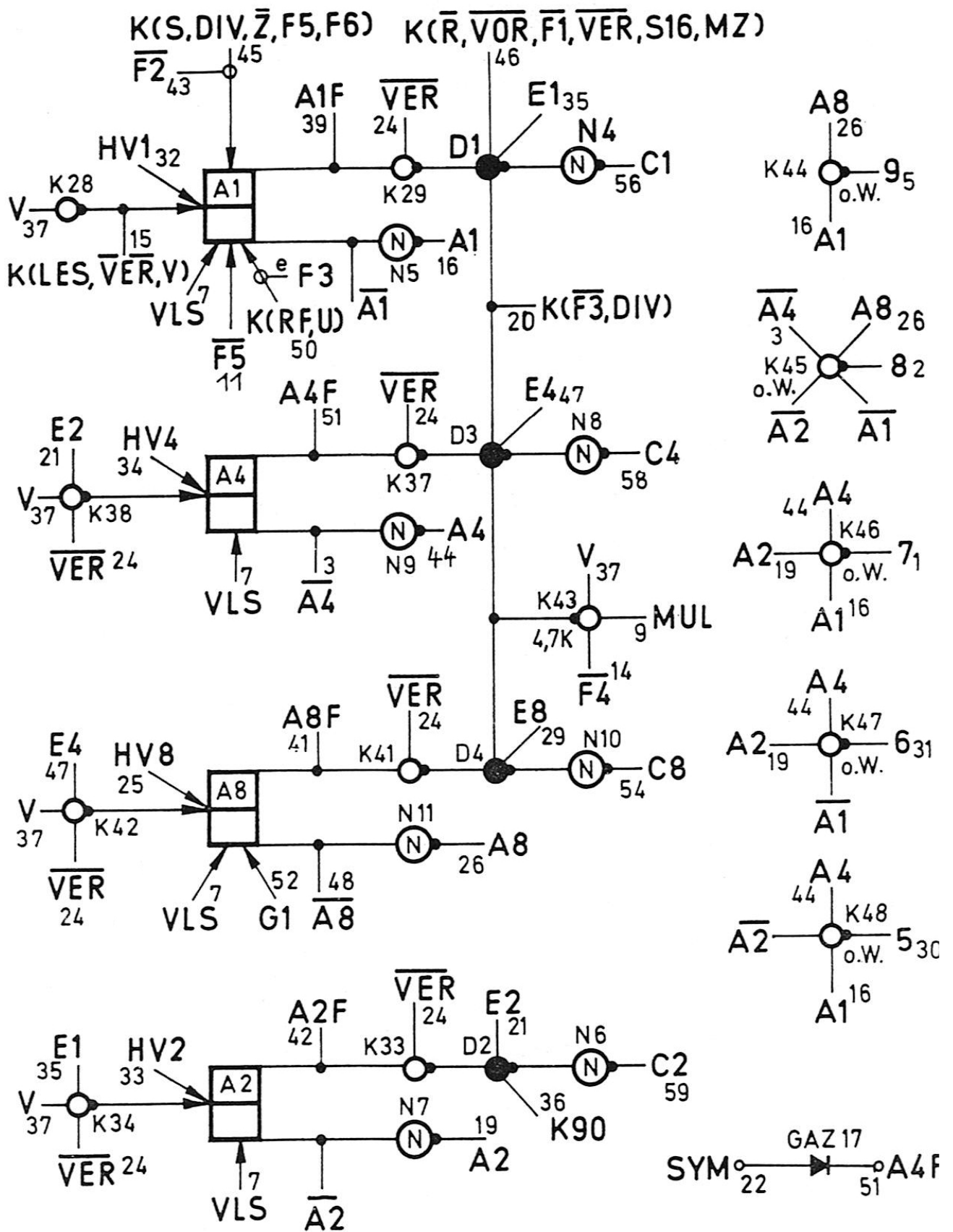
Logic diagram - Board 2



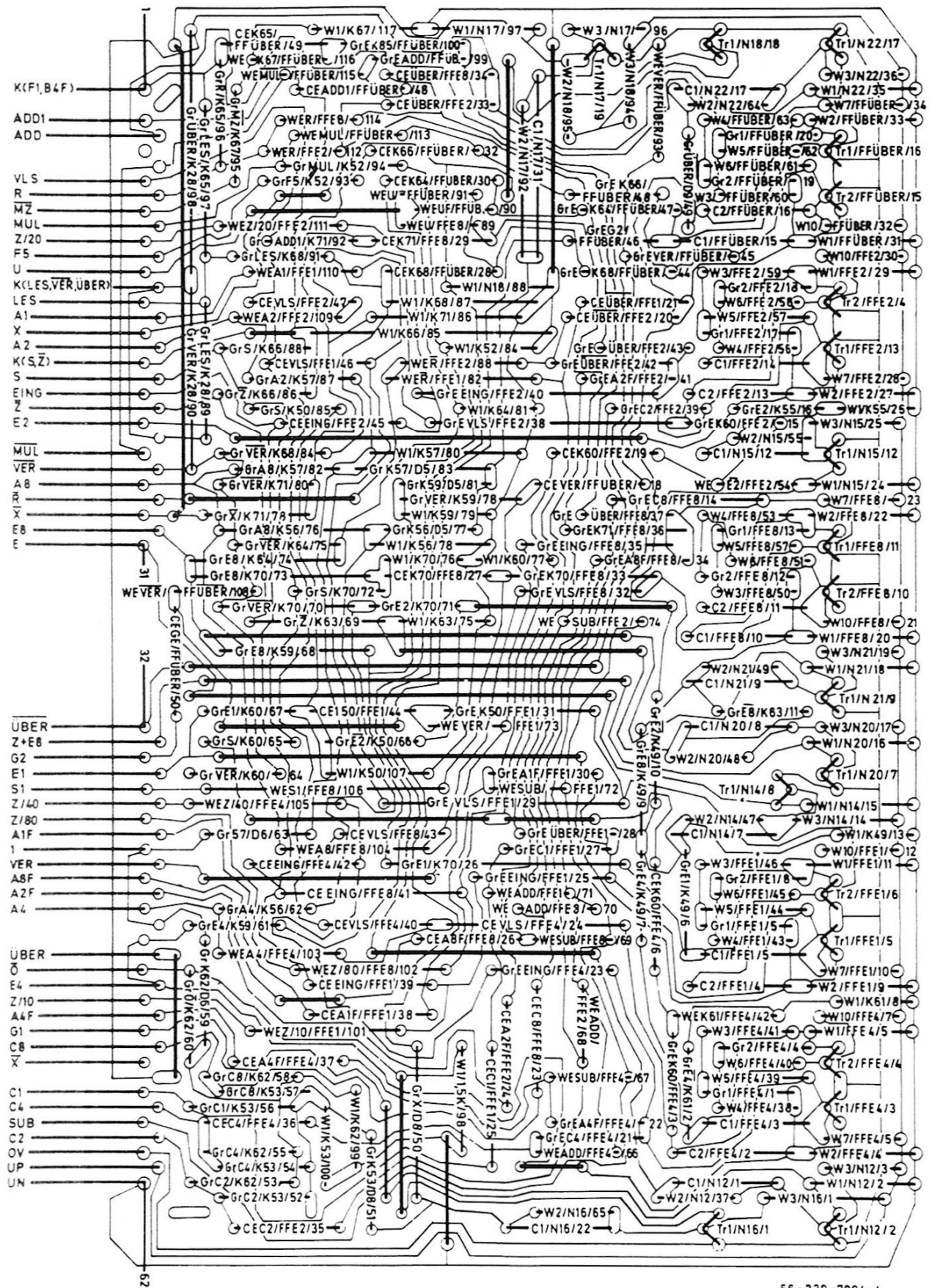
Layout plan - Board 3

1	7	1/12	
2	8	2/12	
3	A	1/1	
4		6/7	
5	9	5/4; 6/12	
6			
7	VLS	7/4/5; 6/8/9/10	
8	F3	8/5/6/7/8/9	5V7
9	MUL	10/4; 11/5/6/7/8/9/10	17V8
10			
11	<u>F5</u>	27/2; 12/5/6/9	
12			
13			
14	<u>F4</u>	13/2; 14/6; 15/9	
15	K28	14/4	
16	AI	15/1; 16/4; 20/8; 19/10	2V8
17			
18			
19	A2	18/1/4	12V8
20	K112	20/6	
21	E2	23/4	13V8
22	SYM	22/6	
23			
24	<u>VER</u>	26/4/5/6/7/8/9/10	
25	HV8	27/1	
26	A8	27/4	32V8
27	<u>B4</u>	27/6/7/9/10	18V7
28	MZ	29/8	
29	E8	30/4	1V7
30	5	30/12	
31	6	31/12	
32	HV1	32/1	
33	FEV2	33/1	
34	HV4	34/1	
35	E1	35/4	3V8
36	K90		
37	V	36/5; 35/6	15V8
38			
39	A1F	39/4	
40	VER	41/4; 40/5; 39/6; 40/8; 41/9	28V8
41	ASF	42/4; 41/7	
42	A2F	43/4; 41/6	
43	<u>F2</u>	43/6; 44/9; 43/10	
44	A4	44/1/4; 45/8	22V8
45	K91	46/5	
46	K152	48/8	
47	E4	49/4	23V8
48	<u>A8</u>	48/1; 34/9	
49	<u>B2</u>	49/7	
50	K132	51/7	
51	A4F	51/4	
52	G1	52/4/8/10	
53	<u>F6</u>	55/6; 56/7; 54/8; 53/9	
54	C8	53/1/2/4	
55			
56	CI	55/1; 56/2/4	
57	\B1\	57/6/7	15V7
58	C4	56/1; 57/4	
59	C2	59/1/4	
60	OV	60/1-12	11.12V2; 5,6V3; 1V8
61	+Up	61/1-12	13V2; 21V7
62	-UN	62/1-12	14,15V2 ; 29V6; 20V7

Pin assignment - Board 3



Logic diagram - Board 3

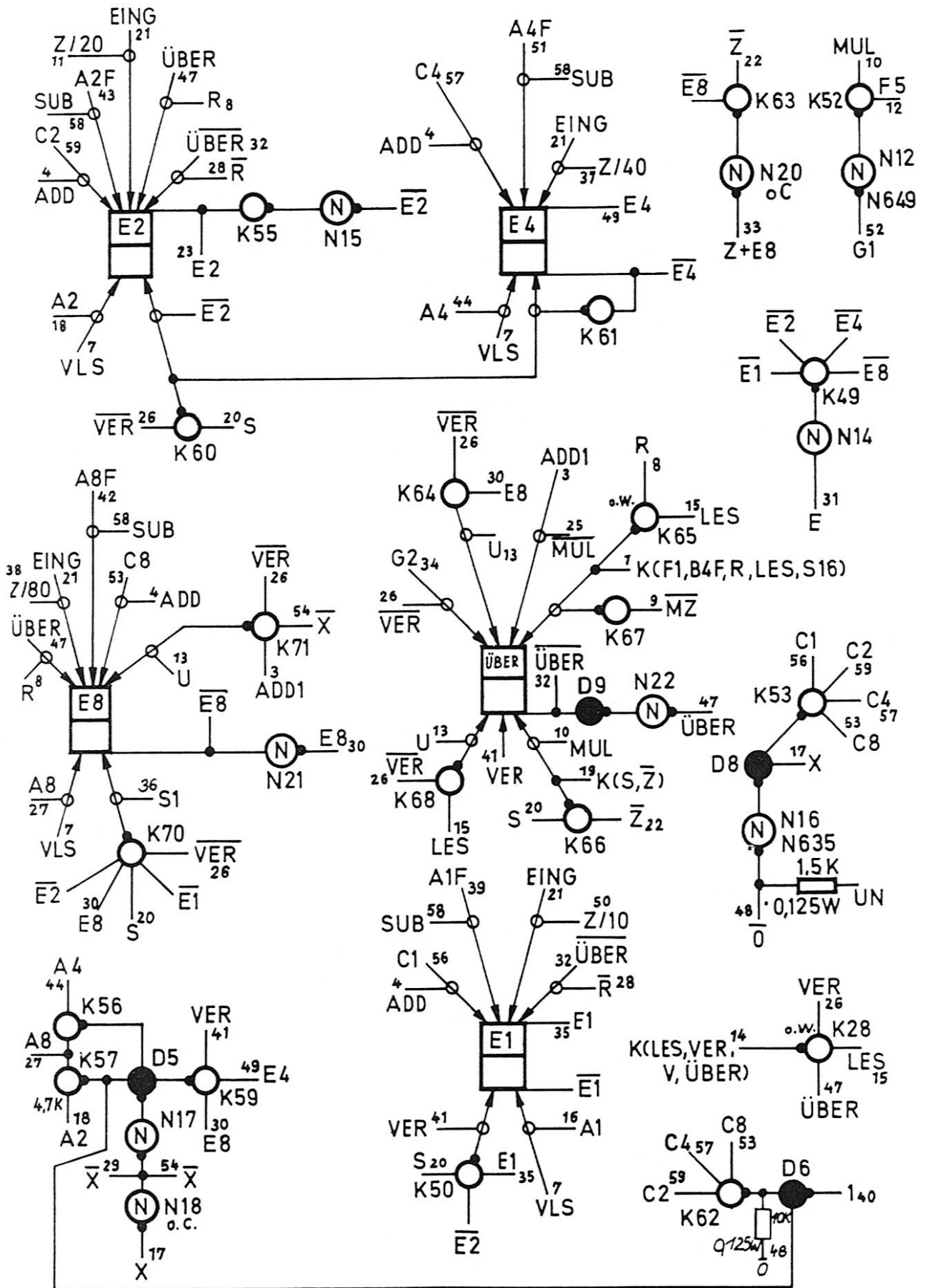


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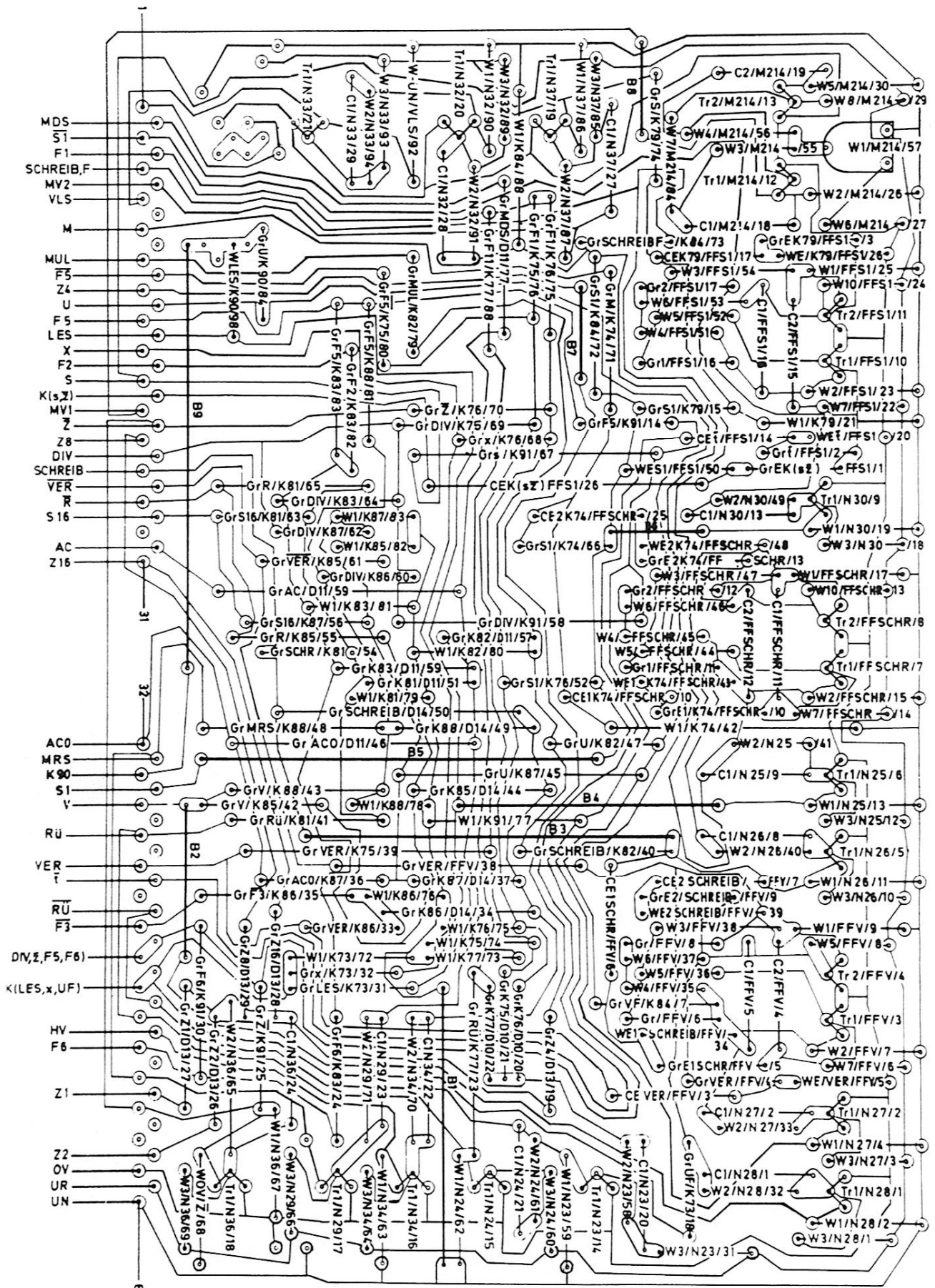
Layout plan - Board 4

1	K65	2/7; 1/8	
2	AU	1/5; 16/12	
3	ADD1	2/6	
4	ADD	3/6/8/9/10	
5	9	5/3; 6/12	
6	MUL		
7	VLS	7/3/5; 6/8/9/10	
8	R	7/6/7/8/9/10	19V8
9	<u>MZ</u>	9/8; 10/9	26V8
10	MUL	9/3; 11/5/6/7/8/9/1	17V8
11	ZI20	22/12	
12	F5	11/2; 15/5/6/7; 14/9/7/7	
13	U	14/5; 13/6/7/8	
14	K28	15/3	
15	LES	15/2; 16/5/6	
16	AI	15/1; 16/3; 20/8; 19/10/2/8	
17	X	17/5; 16/8/9; 13/10	
18	A2	18/1; 19/3	12V8
19	K66	20/5	
20	S	19/5/6; 20/7; 19/8; 20/9	
21	EING	21/7; 22,42/8; 19,43/9	
22	Z	22/5/7; 21/8; 22/9; 20/10	
23	E2	21/3	13V8
24	K28		
25	<u>MUL</u>	25/7/9/10	
26	<u>VER</u>	24/3; 26/5/6/7/8/9/10	
27	A8	26/3	32V8
28	<u>R</u>	27/5; 28/7; 27/8; 28/9/10	
29	<u>X</u>	54/4; 29/5; 30/6/7/8	
30	E8	29/3	1V7
31	E	31/9	
32	<u>UBER</u>	32/8/9	
33	Z+E8	33/7/8/9; 32/10	
34	G2	34/7; 33/10	
35	EI	35/3	3V8
36	Si	36/2; 35/5/7; 34/8/10	7V8
37	ZI40	35/12	
38	ZI80	34/12	
39	A1F	39/3	
40	1	41/12	
41	VER	40/3/5; 39/6; 40/8; 41/9	28V8
42	A8F	41/3/7	
43	A2F	42/3; 41/	
44	A4	44/1/3; 45/8	22V8
45	1		
46	E4		
47	UBER	46/8; 47/9; 46/10	2V7
48	<u>O</u>	49/9; 40/12	
49	E4	47/3	23V8
50	ZI10	42/12	
51	A4F	51/3	
52	G1	52/3/8/10	
53	C8	53/1/2; 54/3	
54	<u>X</u>	29/4/5; 30/6/7/8	
55	UBER		
56	C1	55/1; 56/2/3	
57	C4	56/1; 58/3	
58	SUB	59/6	25V8
59	C2	59/1/3	
60	OV	60/1-12	11,12V2; 5,6V3; 1V8
61	+Up	61/1-12	13V2; 21V7
62	-Un	62/1-12	14,15V2; 29V6; 20V7

Pin assignment - Board 4



Logic diagram - Board 4

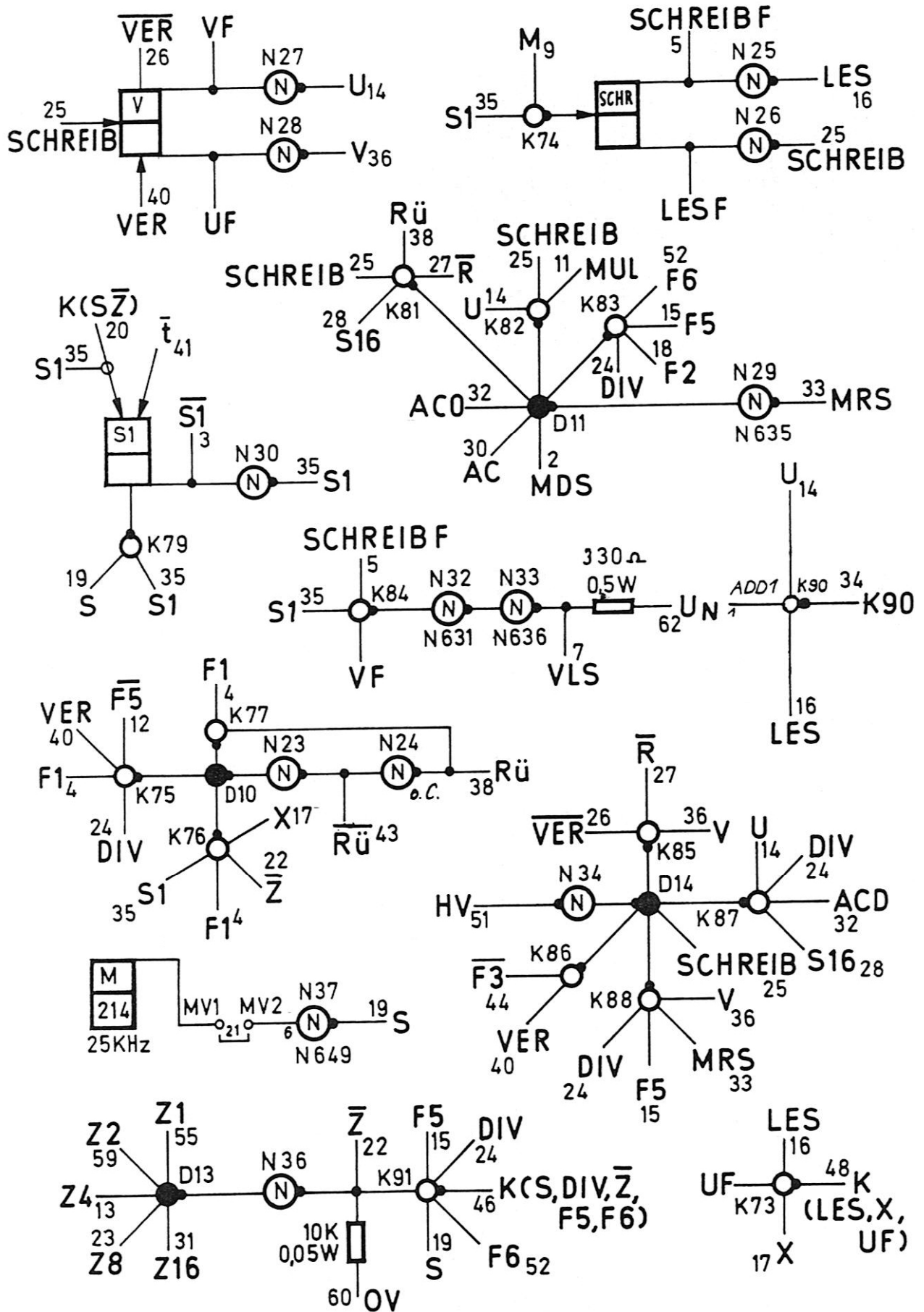


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Layout plan - Board 5

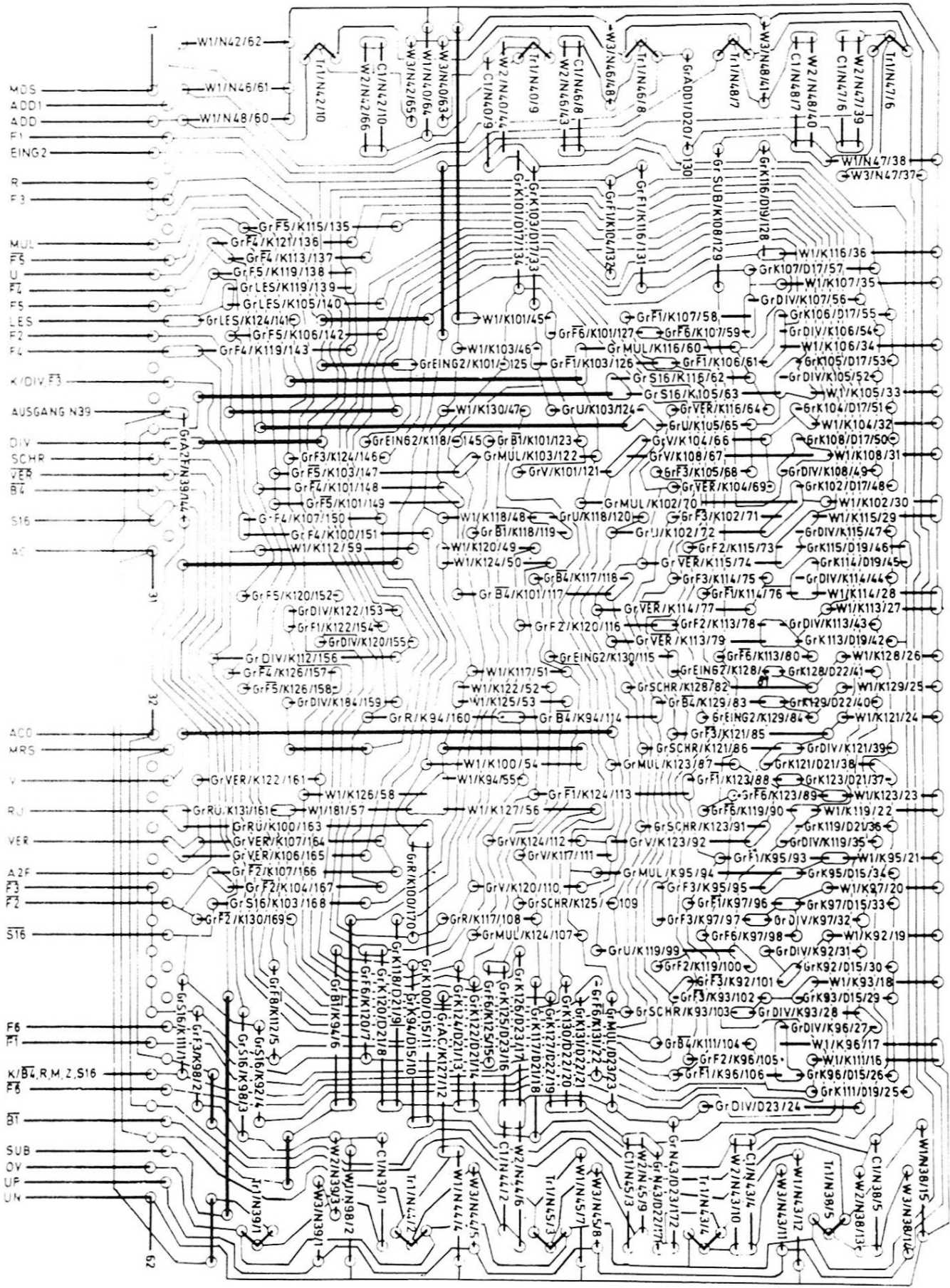
1	AU	2/4; 16/12	
2	MDS	2/2; 1/6	21V8
3	<u>S1</u>	2/8	
4	F1	4/6/7; 5/8; 4/9;- 5/10	3V7
5	SCHRF	5/9	
6	MV`V2	27V7	
7	VLS	7/3/4; 6/8/9/10	
8	F3	8/3/6/7/8/9	5V7
9	<u>M</u>	9/9	6V8
10	<u>ST</u>	9/2; 10/6/7/8; 13/9	
11	MUL	9/3; 10/4; 11/6/7/8/9/10	17V8
12	<u>F5</u>	27/2; 11/3; 12/6/9	
13	Z4	12/2/10; 11/11	11V7
14	U	13/4/6/7/8	
15	F5	11/2; 12/4; 15/6/7; 14/9	7V7
16	LES	15/2/4; 16/6	
17	X	17/4; 16/8/9	
18	F2	17/6; 18/7; 17/8/9	4V7
18	S	19/6; 20/7; 19/8; 20/9	
20	X66	19/4;	
21	MV1	26V7	
22	<u>Z</u>	22/4/7; 21/8; 22/9; 20/10	
23	Z8	18/2; 23/7; 21/10; 23/11	12V7
24	DIV	24/6/7/8/9/10	18V8
25	SCHR	24/1/2; 25/6	5V8
26	<u>VER</u>	24/3; 26/4/6/7/8/9/10	
27	<u>R</u>	28/4/7; 27/8; 28/9/10	
28	S16	29/6/7; 28/8; 29/9/10	
29	<u>X</u>	29,54/4; 30/x/7/8	
30	AC	31/2/6	30V8
31	Z16	31/8/10	13V7
32	ACO	32/2/6	31V8
33	MRS	33/2/6	11V8
34	K9o		
35	S1	36/2/4; 35/7; 34/8/10	7V8
36	V	37/3; 35/6	15V8
37			
38	Rat	37/6; 38/7; 39/8/9; 38/10	27V8
39			
40	VER	40/3; 41/4; 39/6; 40/8; 41/9	28V8
41	<u>t</u>	42/2	
42			
43	<u>RU</u>	41/10	
44	<u>F3</u>	42/6; 43/8	
45	K91		
46	K91	45/3	
47	K73		
48	K73	46/9	
49	<u>RU</u>		
50	RÜ		
51	HV	51/1	20V8
52	P6	51/6; 53/7; 52/9; 50/10	8V7
53			
54	MRS		
55	Z1	54/2; 48/10/11	9V7
56	Z		
57	UV		
58	K(LESF,VF)		
59	Z2	57/2; 54/10; 52/11	10V7
60	OV	60/1-12	11,12V2; 5,6V3; 1V8
61	+Up	61/1-12	13V2; 21V7
62	-Un	62/1-12	14,15V2; 29V6; 20V7

Pin assignment - Board 5



Logic diagram - Board 5

Circuit paths side

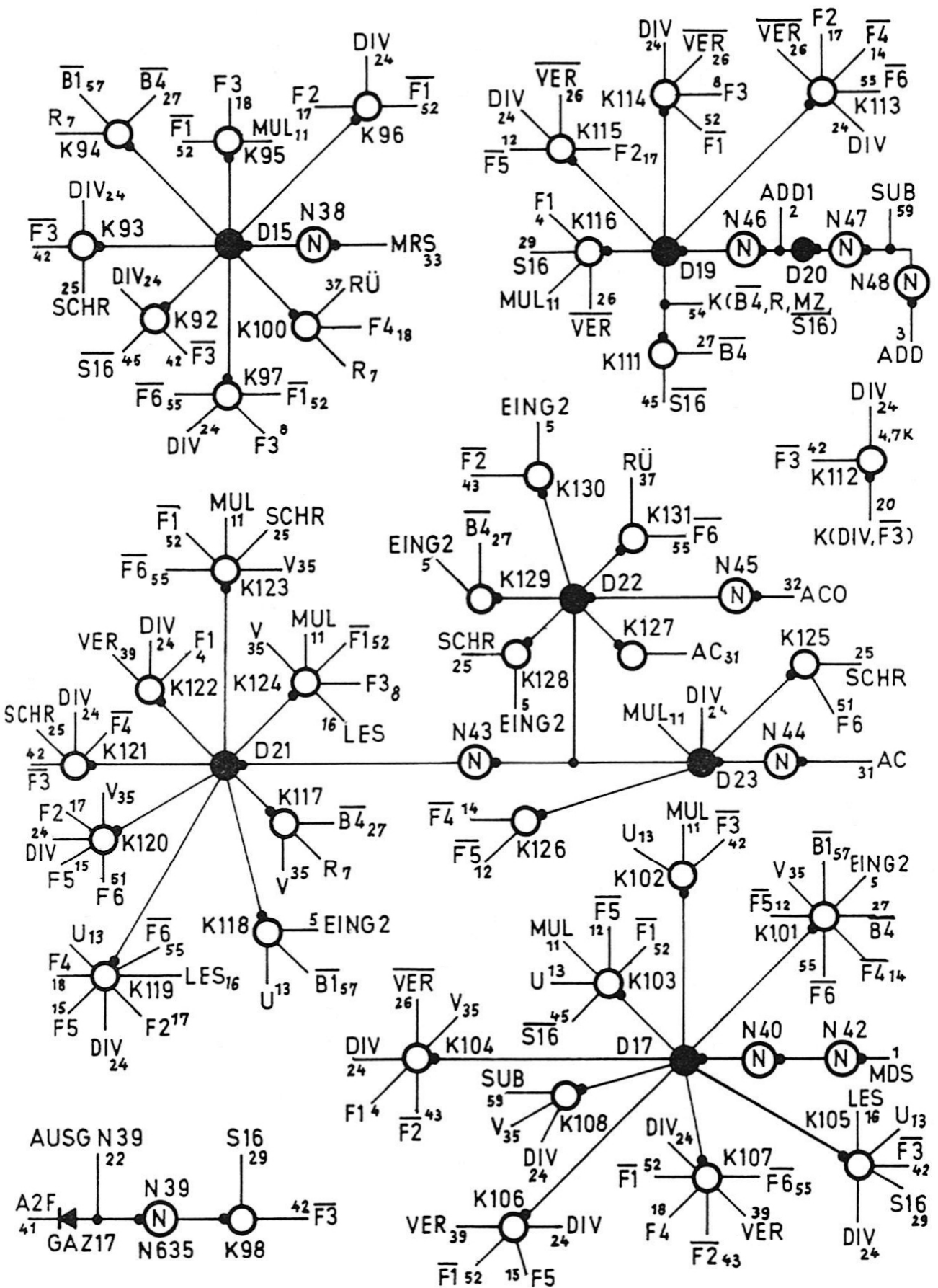


56-220-7006-0

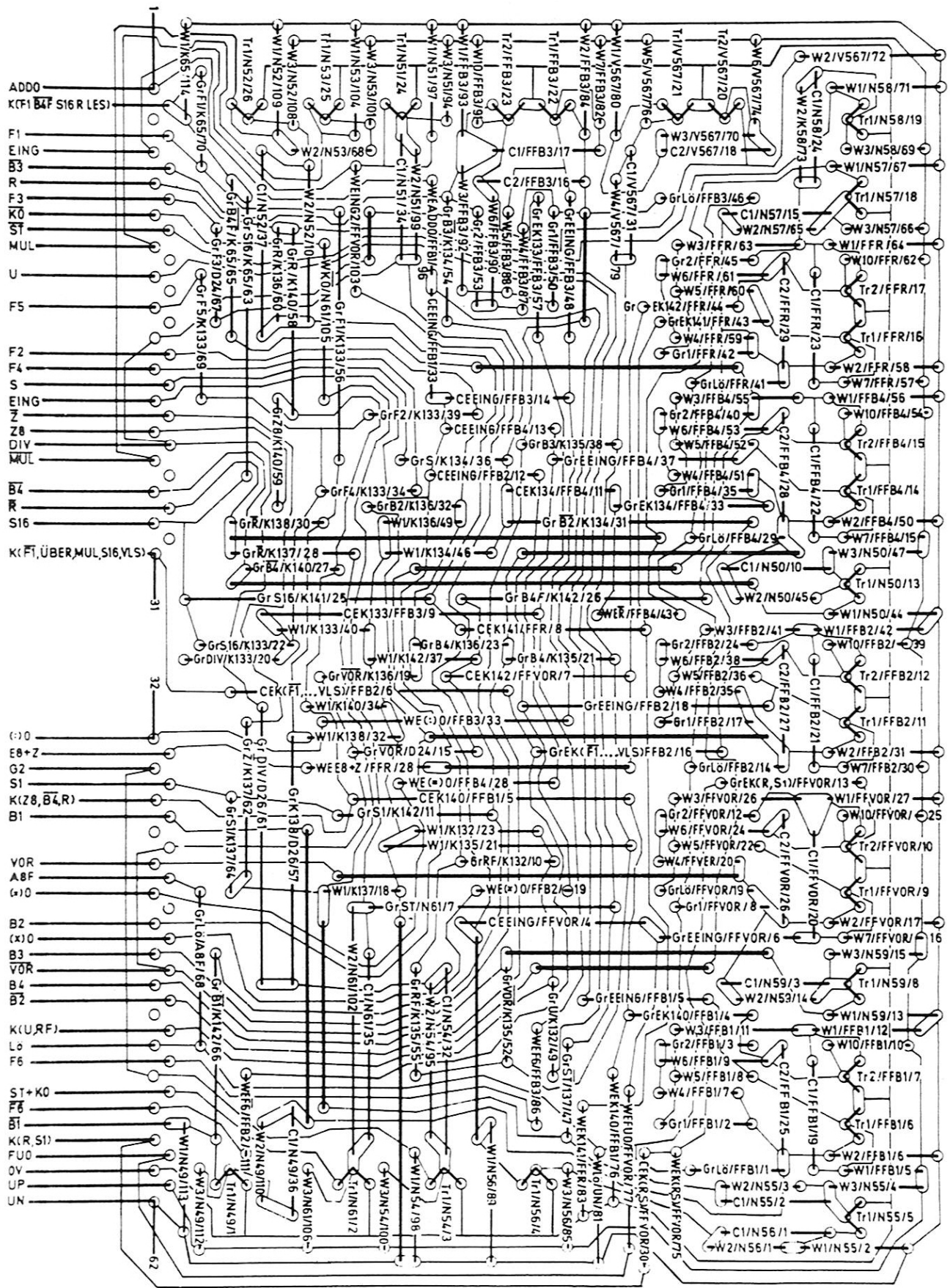
Layout plan - Board 6

1	MDS	2/2/5	21V8
2	ADD1	3/4	
3	ADD	4/4; 3/8/9/10	
4	F1	4/7/7; 5/8; 4/9; 5/10	3V7
5	EING2	5/7	
6			
7	R	8/4; 7/7/8/9/10	19V8
8	F3	8/3/5/7/8/9	5V7
10	<u>ST</u>	9/2; 10/5/7/8; 13/9	
11	MUL	9/3; 10/4; 11/5/7/8/9/10/17V8	
12	<u>F5</u>	27/2; 11/3; 12/5/9	
13	U	13/4; 14/5; 13/7/8	
14	<u>F4</u>	13/2; 14/3; 15/9	
15	F5	11/2; 12/4; 15/5/7; 14/9	7V7
16	LES	15/2/4; 16/5	
17	F2	18/5/7; 17/8/9	4V7
18	F4	14/2; 19/7; 18/9	6V7
19	S	20/4; 19/5; 20/7; 19/8; 20/9	
20	K112	20/3	
21			
22	SYM	22/3	
23	S16		
24	DIV	24/5/7/8/9/10	18V8
25	SCHR	24/1/2; 25/5	5V8
26	<u>VER</u>	24/3; 26/4/5/7/8/9/10	
27	<u>B4</u>	27/3/7/9/10	18V7
28			
29	S16	28/5; 29/7; 28/8; 29/9/10	
30	<u>X</u>	29,54/4; 29/5; 30/7/8	
31	AC	31/2; 30/5	30V8
32	ACO	32/2/5	31V8
33	MRS	33/2/5	11V8
34			
35	V	37/3; 36/5	15V8
36	B1	37/7	
37	RU	38/5/7; 39/8/9; 38/10	27V8
38			
39	VER	40/3; 42/4; 40/5/8; 41/9	28V8
40			
41	A2F	42/3; 43/4	
42	<u>F3</u>	44/5; 43/8	
43	<u>F2</u>	43/3; 44/9; 43/10	
44	<u>F3</u>		
45	<u>S16</u>	45/10	
46	<u>F3</u>		
47			
48			
49			
50			
51	F6	52/5; 53/7; 52/9; 50/10	8V7
52	<u>F1</u>	50/8; 51/10	
53	MRS		
54	K111	53/8	
55	<u>F6</u>	53/3; 56/7; 54/8; 53/9	
56	ACO		
57	B1	57/3/7	15V7
58	AC		
59	SUB	58/4	25V8
60	OV	60/1-12	11,12V2; 5,6V3; 1V8
61	+Up	61/1-12	13V2; 21V7
62	-Un	62/1-12	14,15V2; 29V6; 20V7

Pin assignment - Board 6



Logic diagram - Board 6

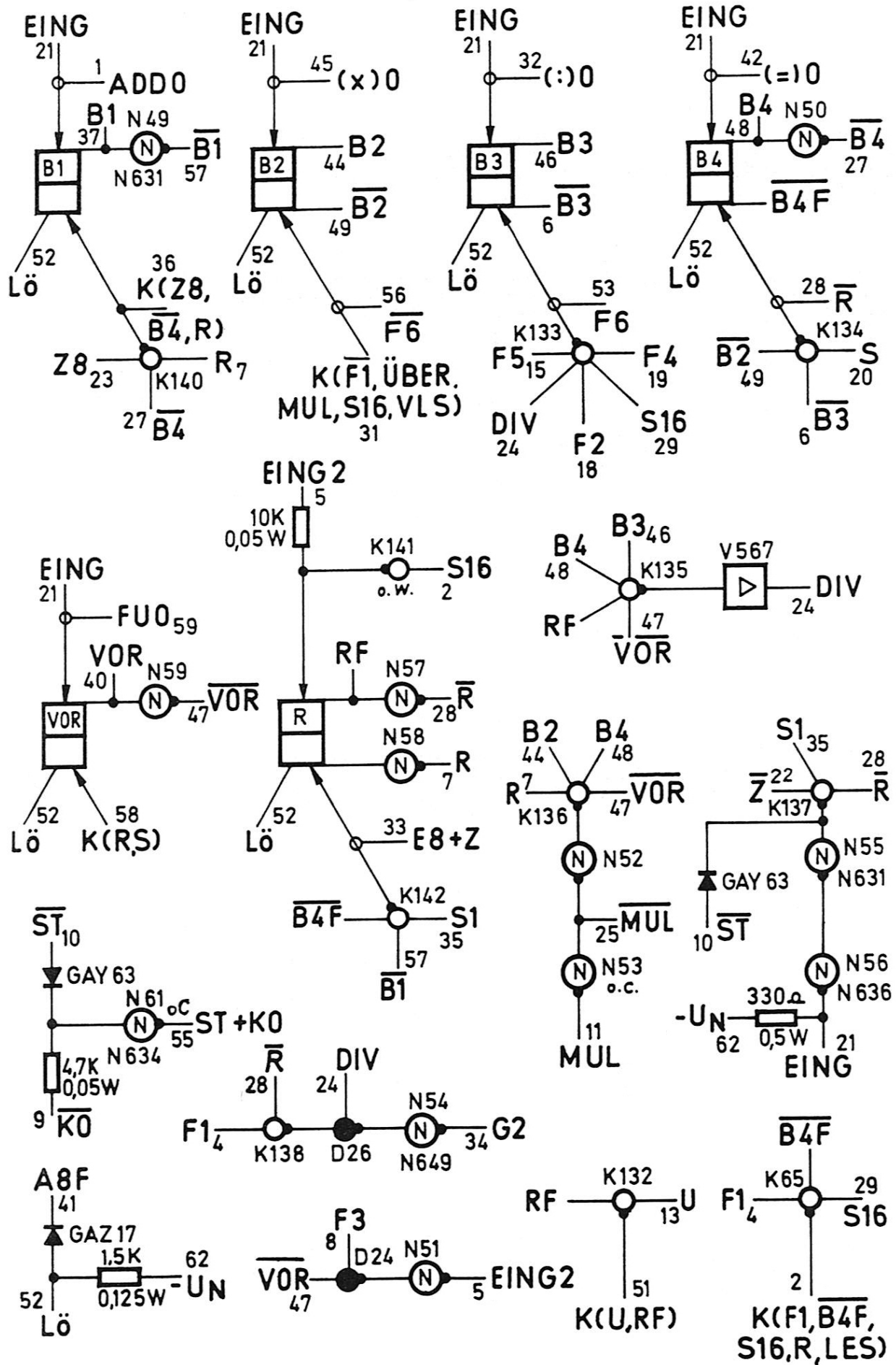


56-220-7007/7

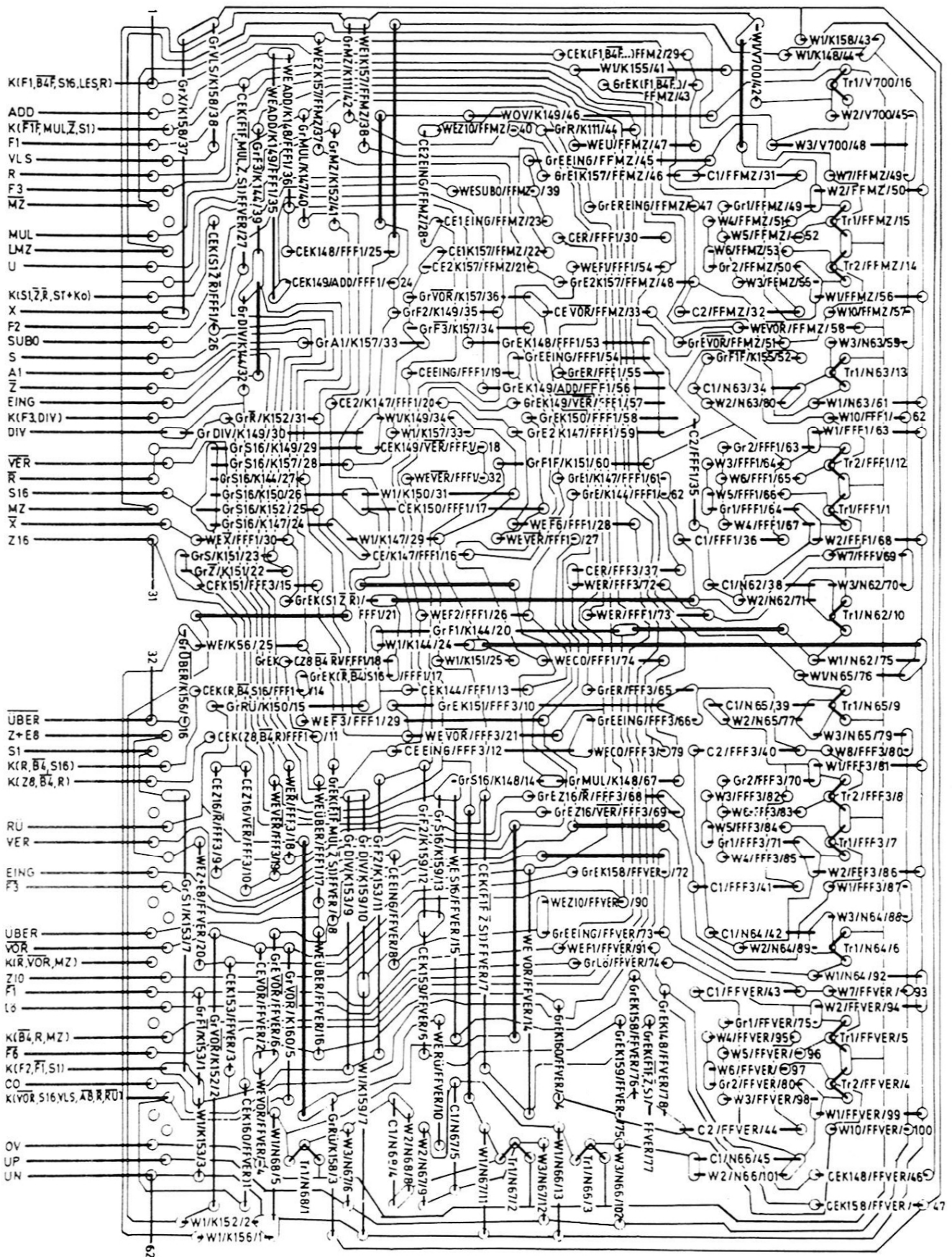
Layout plan - Board 7

1	ADDO	1/11	
2	K65	1/4/8	
3			
4	F1	4/5/6; 5/8; 4/9; 5/10	3V7
5	EING2	5/6	
6	$\overline{B3}$	4/3	
7	R	8/4; 7/6/8/9/10	19V8
8	F3	8/3/5/6/8/9	5V7
9	\overline{KO}	44/8; 45/9	
10	\overline{ST}		
11	MUL	9/3; 10/4; 611/5/6/8/9/10	17V8
12			
13	U	13/4; 14/5; 13/6/8	
14			
15	F5	11/2; 12/4; 15/5/6; 14/9	7V7
16			
17	DIV		
18	F2	18/5; 17/6/8/9	4V7
19	F4	14%2; 18/6/9	6V7
20	S	20/4; 19/5/6/8; 20/9	
21	EING	21/4; 22,42/8; 19,43/9	
22	\overline{Z}	22/4/5; 21/8; 22/9; 20/10	
23	Z8	18/2; 23/5; 21/10; 23/11	12V7
24	DIV	24/5/6/8/9/10	18V8
25	\overline{MUL}	25/4/9/10	
26	\overline{VER}	24/3; 26/4/5/6/8/9/10	
27	$\overline{B4}$	27/3/6/9/10	18V7
28	\overline{R}	28/4; 27/5/8; 28/9/10	
29	S16	28/5; 29/6; 28/8; 29/9/10	
30	\overline{X}	29,54/4; 29/5; 30/6/8	
31	K182	30/10	
32	:O	32/11	
33	Z+E8	33/4/8/9; 32/10	
34	G2	34/4; 33/10	
35	S1	36/2/4; 35/5; 34/8/10	7V8
36	K140	36/8	
37	B1	36/6	
38	RU	38/5; 37/6; 39/8/9; 38/10	27V8
39	\overline{VOR}		
40	VOR		
41	A8F	41/3; 42/4	
42	=0	43/11	
43			
44	B		16V7
45	(x)0	45/11	
46	B3		
47	\overline{VOR}	47/8	29V8
48	B4		
49	B2	49/3	
50	DRUCK K		
51	K132	50/3	
52	Lö	51/8; 50/9	31V4
53	F6	52/5; 51/6; 52/9; 50/10	8V7
54			
55	ST+KO	53/10	
56	$\overline{F6}$	53/3; 55/6; 54/8; 53/9	
57	$\overline{B1}$	57/3/6	15V7
58	K194	59/10	
59	FUO	59/9/11	
60	OV	60/1-12	11,12V2; 5,6V3; 1V8
61	+Up	61/1-12	13V2; 21V7
62	-Un	62/1-12	14,15V2; 29V6; 20V7

Pin assignment - Board 7

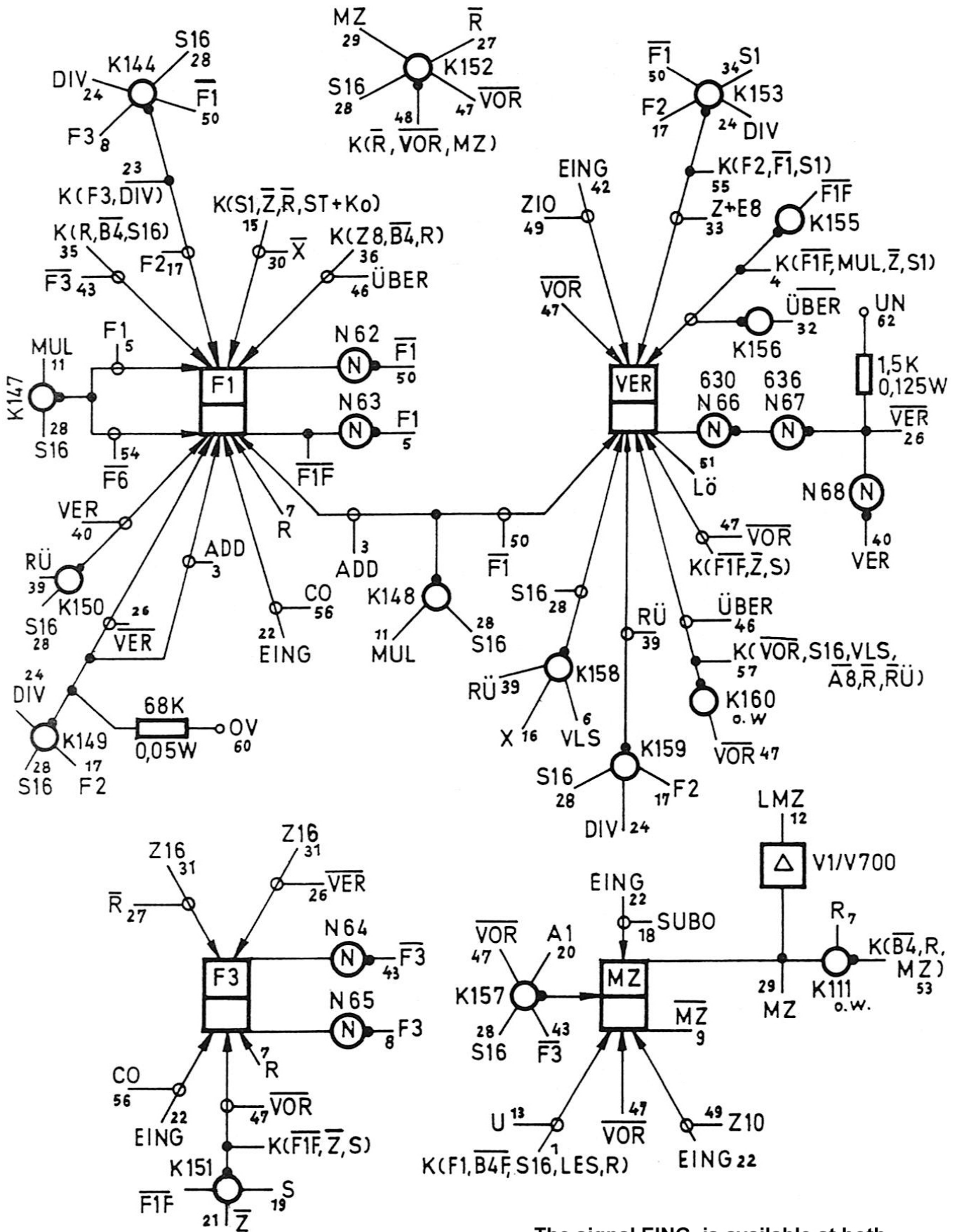


Logic diagram - Board 7



1	K65	1/4; 2/7	
2	<u>SI</u>	3/5'	
3	ADD	4/4; 3/6/9/10	
4	K155	4/10	
5	F1	4/5/6/7/9. 5/10	3V7
6	VLS	7/3/4/5; 6/9/10	
7	R	8/4; 7/7/9/10	19V8
8	F3	8/3/5/6/7/9	5V7
9	<u>MZ</u>	9/4; 10/9	26V8
10	<u>ST</u>	9/2; 10/5/6/7; 13/9	
11	MUL	9/3; 10/4; 11/5/6/7/9/10	17V8
12	LMZ		28V6
13	U	13/4; 14/5; 13/6/7	
14	MZ		
15	K186	14/10	
16	X	17/4/5; 16/9; 13/10	
17	F2	18/5; 17/6; 18/7; 17/9	4V7
18	SUBO	18/11	
19	S	20/4; 19/5/6; 20/7/9	
20	AI	15/1; 16/3/4; 19/10	2V8
21	<u>Z</u>	22/4/5/7/9; 20/10	
22	EING	21/4/7; 42/8; 19,43/9	
23	K144	23/9	
24	DIV	24/5/6/7/9/10	18V8
26	<u>VER</u>	24/3; 26/4/5/6/7/9/10	
27	<u>R</u>	28/4; 27/5; 28/7/9/10	
28	S16	28/5; 29/6/7/9/10	
29	MZ	28/3	
30	<u>X</u>	29,54/4; 29/5; 30/6/7	
31	Z16	31/5/10	13V7
32	<u>UBER</u>	32/4/9	
33	Z+E8	33/4/7/9; 32/10	
34	S1	36/2/4; 35/5/7; 34/10	7V8
35	K183	35/10	
36	K140	36/7	
37	S1		
38			
39	RU	38/5; 37/6; 38/7; 39/9; 38/10	2778
40	VER	40/3; 41/4; 40/5; 39/6; 41/9	28V8
41	Z+E8		
42	EING	21/4/7; 22/8; 19,43/9	
43	<u>F3</u>	44/5; 42/6	
44	<u>KO</u>	9/7; 45/9	
45	A4	44/1/3/4	22V8
46	<u>ÜBER</u>	47/4/9; 46/10	2V7
47	<u>VOR</u>	47/7	29V8
48	K152	46/3	
49	Z10	48/9; 49/12	
50	<u>F1</u>	52/6; 51/10	
51	Lö	52/7; 50/9	31V4
52	G1	52/3/4/10	
53	K111	54/6	
54	FT	53/3; 55/6; 56/7; 53/9	
55	K153	54/9	
56	CO	57/12	
57	K160	57/9/10	
58	UV		
59	K(LESF,VF)		
60	OV	60/1-12	11,12V2; 5,673; 1V8
61	+Up	61/1-12	13V2; 21V7
62	-Un	62/1-12	14,15V2; 29V6; 20V7

Pin assignment - Board 8

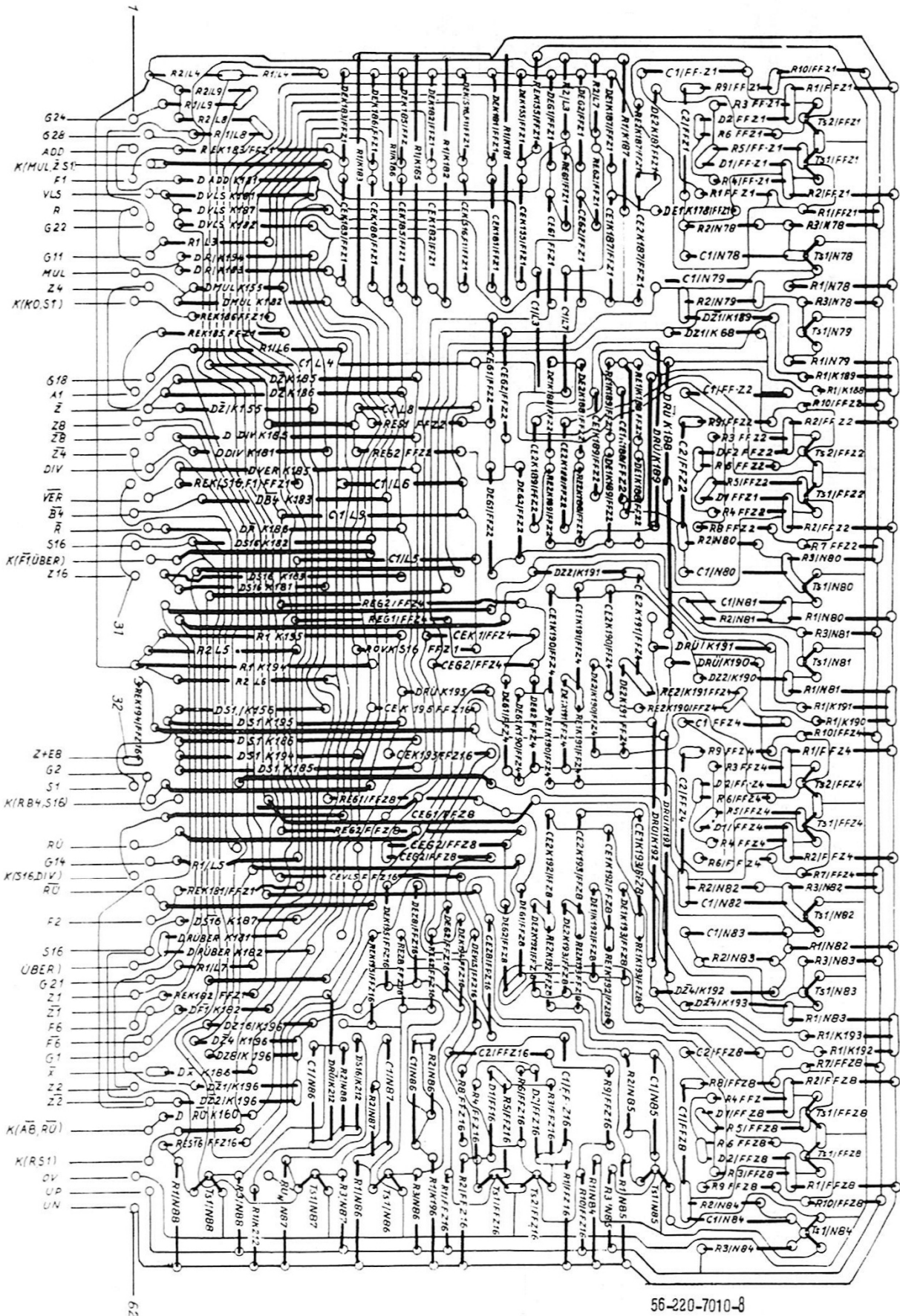


The signal EING, is available at both connector pins 22 and 42

Logic diagram - Board 8

1	K162	1/2	
2	(±)0	3/11	
3	ADD	4/4; 3/6/8/10	
4	F1	4/5/6/7; 5/8/10	3V7
5	SCHRF	5/5	
6	VLS	7/3/4/5; 6/8/10	
7	R	8/4; 8/3/5/6/7/8	19V8
8	F3	8/3/5/6/7/8	5V7
9	M	9/5	6V8
10	<u>MZ</u>	9/4/8	26V8
11	MUL	9/3; 10/4; 11/5/6/7/8/10	17V8
12	<u>F5</u>	27/2; 11/3; 12/5/6	
13	ST	9/2; 10/5/7/8	
14	F5	11/2; 12/4; 15/5/6/7	7V7
15	<u>F4</u>	13/2; 14/3/6	
16	X	17/4/5; 16/8; 13/10	
17	F2	18/5; 17/6; 18/7; 17/8	4V7
18	F4	14/2; 18/6; 19/7	6V7
19	EING	21/4/7; 22,42/8;43/9	
20	S	20/4; 19/5/6; 20/7; 19/8	
21	DIV 01k	9V5	
22	<u>Z</u>	22/4/5/7; 21/8; 20/10	
23	K144	23/8	
24	DIV	24/5/6/7/8/10	18V8
25	<u>MUL</u>	25/4/7/10	
26	<u>VER</u>	24/3; 26/4/5/6/7/8/10	
27	<u>B4</u>	27/3/6/7/10	18V7
28	<u>R</u>	28/4; 27/5; 28/7; 27/8; 28/10	
29	S16	28/5; 29/6/7; 28/8; 29/10	
30	<u>K</u>	7V3	
31	<u>E</u>	31/4	
32	<u>UBER</u>	32/4/8	
33	Z+E8	33/4/7/8; 32/10	
34	A8	48/1/3	
35			
36			
37			
38			
39	RÜ	38/5; 37/6; 38/7; 39/8; 38/10	27V8
40	K169	40/10	
41	VER	40/3; 41/4; 40/5; 39/6; 40/8	28V8
42	#(*)0	44/11	
43	EING	21/4/7; 22,42/8; 19/9	
44	<u>F2</u>	43/3/6/10	
45	<u>KO</u>	9/7; 44/8	
46	K73	48/5	
47	ÜBER	47/4; 46/8/10	2V7
48	ZIO	49/8/12	
49	<u>O</u>	48/4; 40/12	
50	Lö	52/7; 51/8	31V4
51	K160		
52	F6	52/5; 51/6; 53/7; 50/10	8V7
53	<u>F6</u>	3/3; 55/6; 56/7; 54/8	
54	K153	55/8	
55	(II)0	53/11	
56	(I)0	54/11	
57	K160	57/8/10	
58			
59	FUO	59/7/11	
60	0V	60/1-12	11,12V2; 5,6V3; 1 V8
61	+Up	61/1-12	13V2; 21V7
62	-Un	62/1-12	14,15V2; 29V6; 20V7

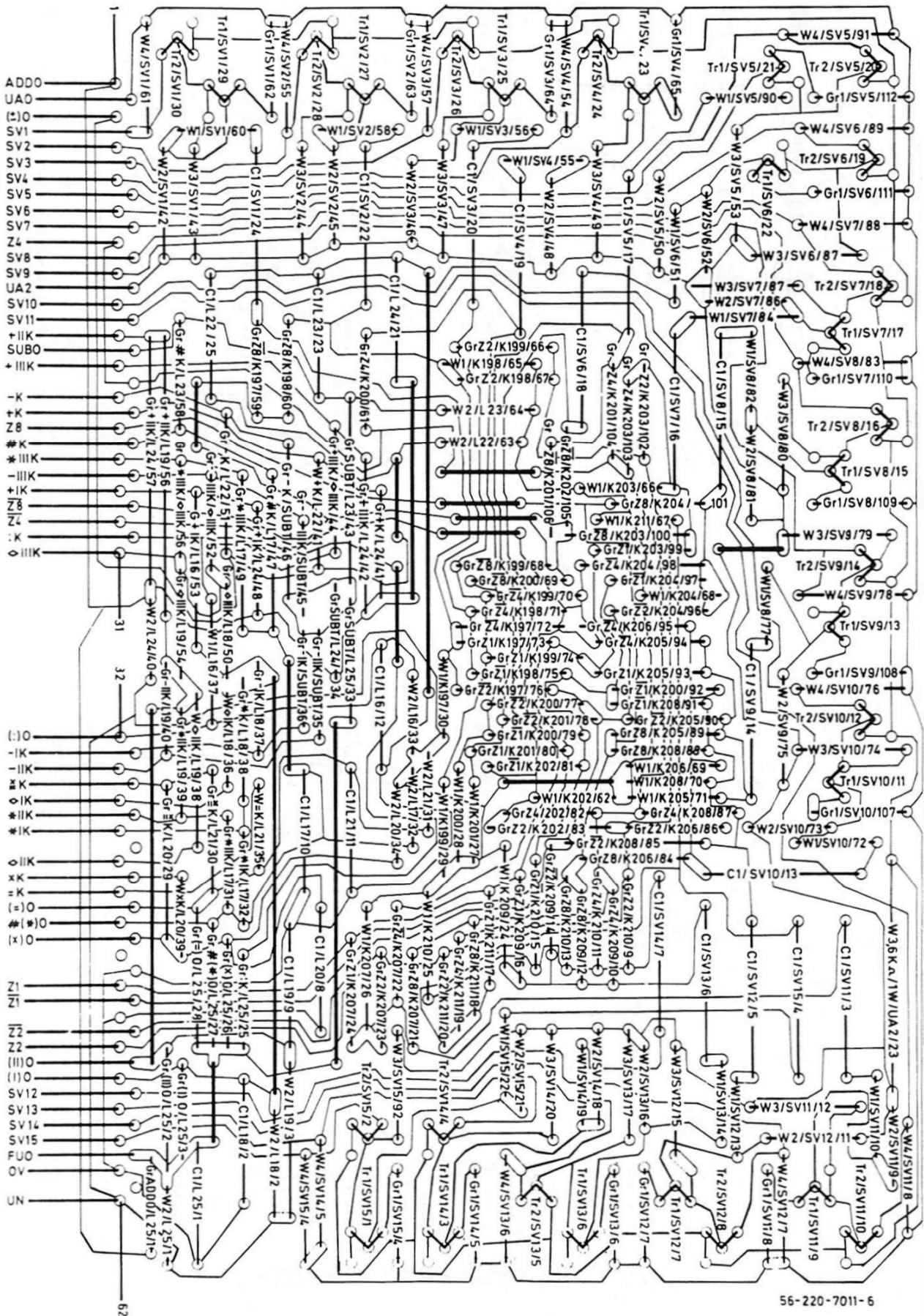
Pin assignment - Board 9



Layout plan - Board 10

1	G24		6V5
2	G28		7V5
3	ADD	4/4; 3/6/8/9	
4	K155	4/8	
5	F1	4/5/6/7; 5/8; 4/9	3V7
6	VLS	7/3/4/5; 6/8/9	
7	R	8/4; 7/6/7/8/9	19V8
8	G22		5V5
9			
10	G11		1V5
11	MUL	9/3; 10/4; 11/5/6/7/8/9	17V8
12	Z4	12/2; 13/5; 11/11	11V7
13	X	17/4/5; 16/8/9	
14	K186	15/8	
15			
16			
17			
18	G18		3V5
19	A1	15/1; 16/3/4; 20/8	2V8
20	\overline{Z}	22,4/5/7; 21/8; 22/9	
21	Z8	18/2; 23/5/7/11	12V7
22	$\overline{Z8}$	29/2; 28/11	
23	Z4	30/2; 29/11	
24	DIV	24/5/6/7/8/9	18V8
25	\overline{MUL}	25/4/7/9	
26	\overline{VER}	24/3; 26/4/5/6/7/8/9	
27	$\overline{B4}$	27/3/6/7/9	18V7
28	\overline{R}	28/4; 27/5; 28/7; 27/8; 28/9	
29	S16	28/5; 29/6/7; 28/8; 29/9	
30	K182	31/7	
31	Z16	31/5/6/	13V7
32	Z+E8	33/4/5/7/9	
33	G2	34/4/7	
34	S1	36/2/4; 35/5/7; 34/8	7V8
35	K183	35/8	
36			
37			
38	Ru	38/5; 37/6; 38/7; 39/8/9	27V8
39	G14	2V5	
40	K169	40/9	
41	\overline{RU}	43/5	
42			
43	$\overline{F2}$	43/3/6; 44/9	
44			
45	$\overline{S16}$	45/6	
46	uBER	47/4; 46/8; 47/9	2V7
47	G21		4V5
48	Z1	54/2; 55/5; 48/11	9V7
49	$\overline{Z1}$	58/2; 49/11	
50	F6	52/5; 51/6; 53/7; 52/9	8V7
51	$\overline{F1}$	52/6; 50/8	
52	G1	52/3/4/8	
53	ST+KO	55/7	
54	Z2	57/2; 59/5; 52/11	10V7
55	$\overline{Z2}$	59/2; 51/11	
56			
57	K160	57/8/9	
58			
59	K194	58/7	
60	0V	60/1-12	11,12V2; 5,6V3; 1V8
61	+Up	61/1-12	13V2; 21V7
62	-Un	62/1-12	14,15V2; 29V6; 20V7

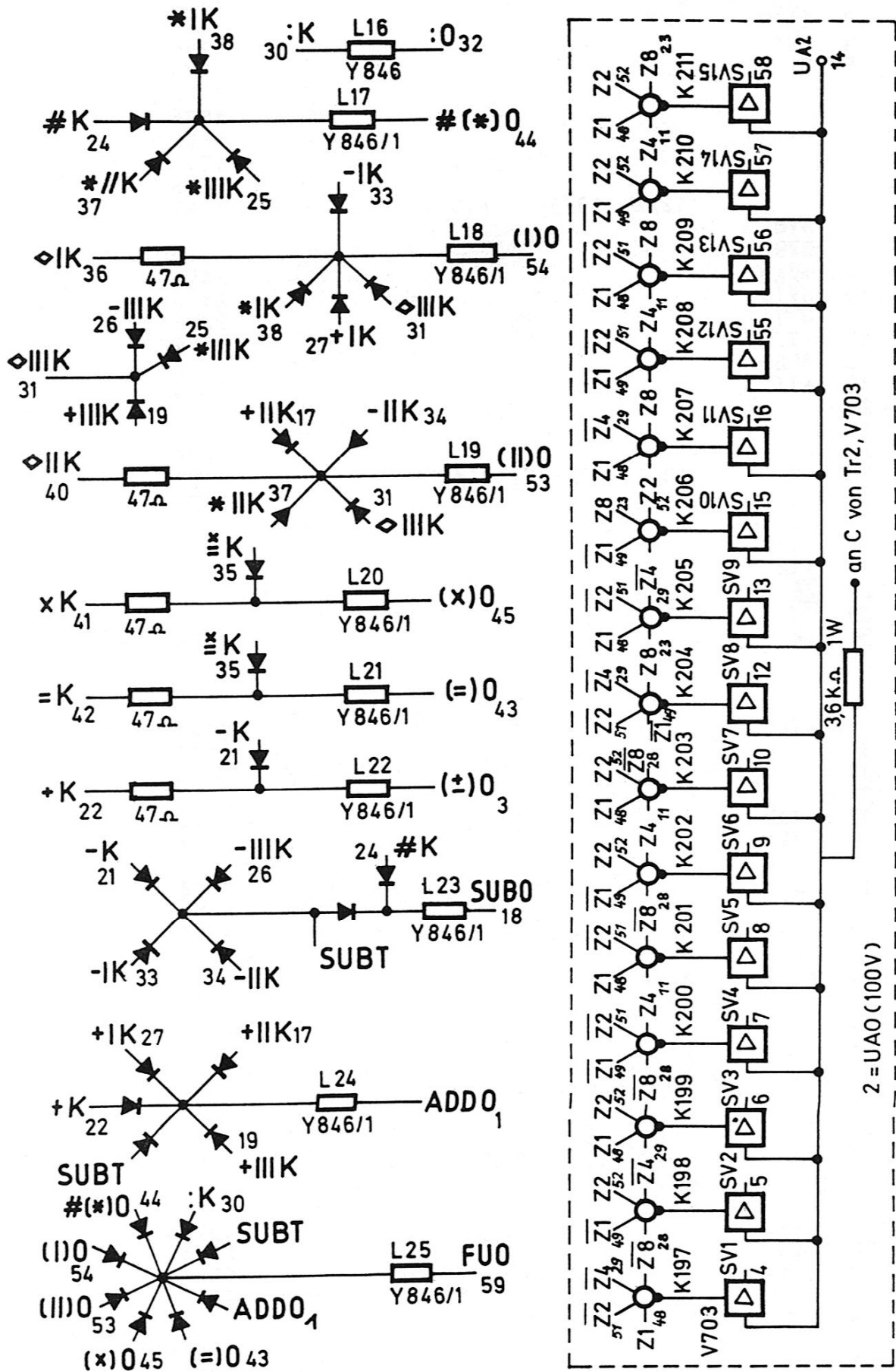
Pin assignment - Board 10



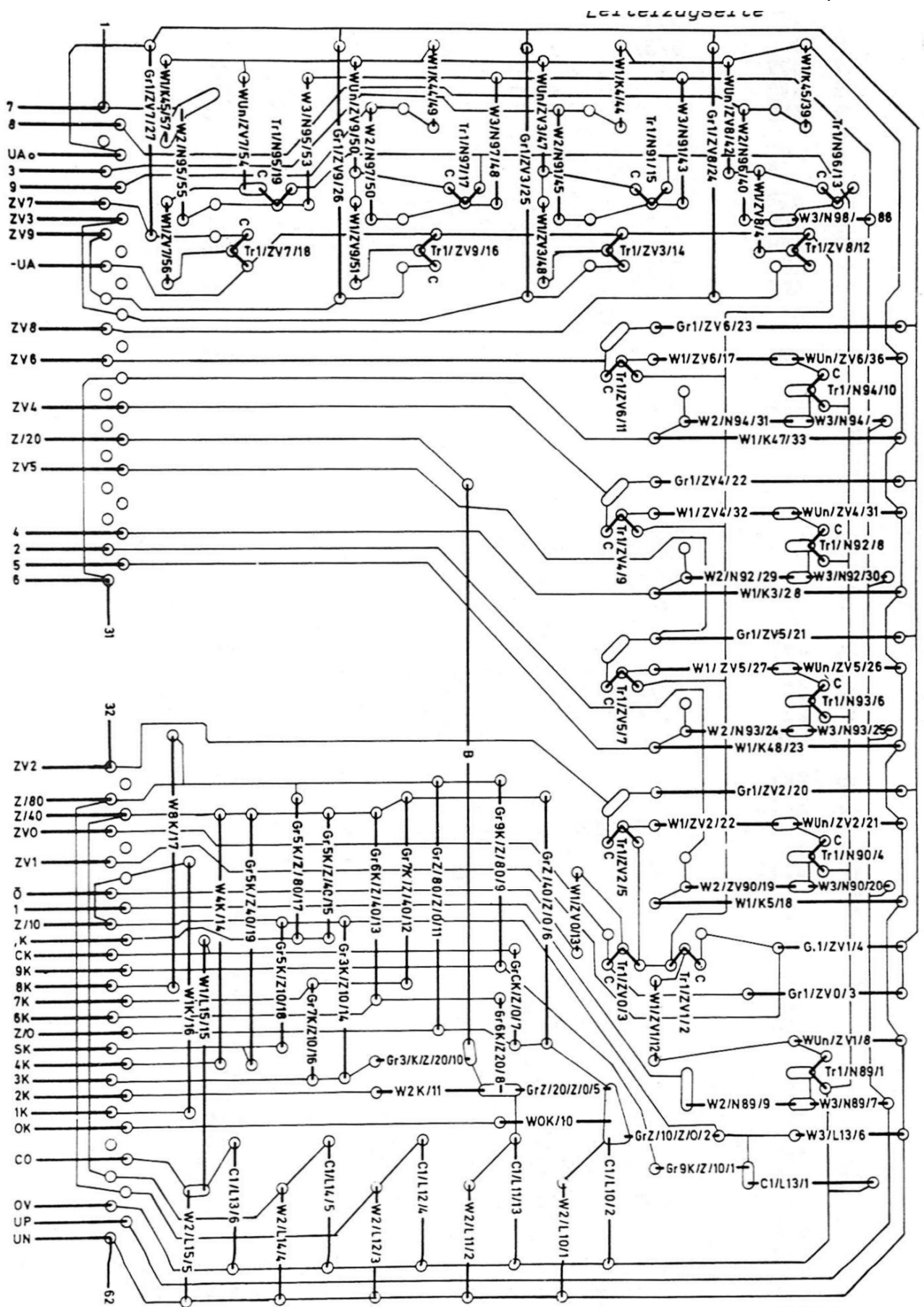
Layout plan - Board 11

1	ADDO	1/7	
2	UAO	4/12	8V2
3	(±)0	2/9	
4	SV1		12V6
5	SV2		13V6
6	SV3		14V6
7	SV4		15V6
8	SV5		16V6
9	SV6		17V6
10	SV?		18V6
11	Z4	12/2; 13/5; 12/10	11V7
12	SV8		19V6
13	SV9		20V6
14	+UA2		24V7
15	SV10		21V6
16	SV11		22V6
17	+IIk		20V4
18	SUB0	18/8	
19	+IIIk	21V4	
20	Z4		
21	-k	13V4	
22	+k	12V4	
23	Z8	18/2; 23/5/7; 21/10	12V7
24	#k	20V3	
25	*IIIk	27V4	
26	-IIIk	24V4	
27	+Ik		19V4
28	$\overline{Z8}$	29/2; 22/10	
29	$\overline{Z4}$	30/2; 23/10	
30	:k	15V4	
31	<>IIIk	30V4	
32	:0	32/7	
33	-Ik		22V4
34	-IIk		23V4
35	xnk		16V4
36	<>Ik		28V4
37	*IIk		26V4
38	*Ik		25V4
39			
40	<>11k	29V4	
41	xk		14V4
42	=k		17V4
43	(=)0	42/7	
44	(*)0	42/9	
45	(x)0	45/7	
46			
47	0V		
48	Z1	54/2; 55/5; 48/10	9V7
49	$\overline{Z1}$	58/2; 49/10	
50	0V		
51	$\overline{Z2}$	59/2; 55/10	
52	Z2	57/2; 59/5; 54/10	10V7
53	(II)0	45/9	
54	(I)0	56/9	
55	SV12		23V6
56	SV13		24V6
57	SV14		25V6
58	SV15		26V6
59	FUO	59/7/9	
60	0V	60/1-12	11,12V2; 5,6V3; 1V8
61	+Up	61/1-12	13V2; 21V7
62	-UP1	62/1-12	14,15V2; 29V6; 20V7

Pin assignment - Board 11



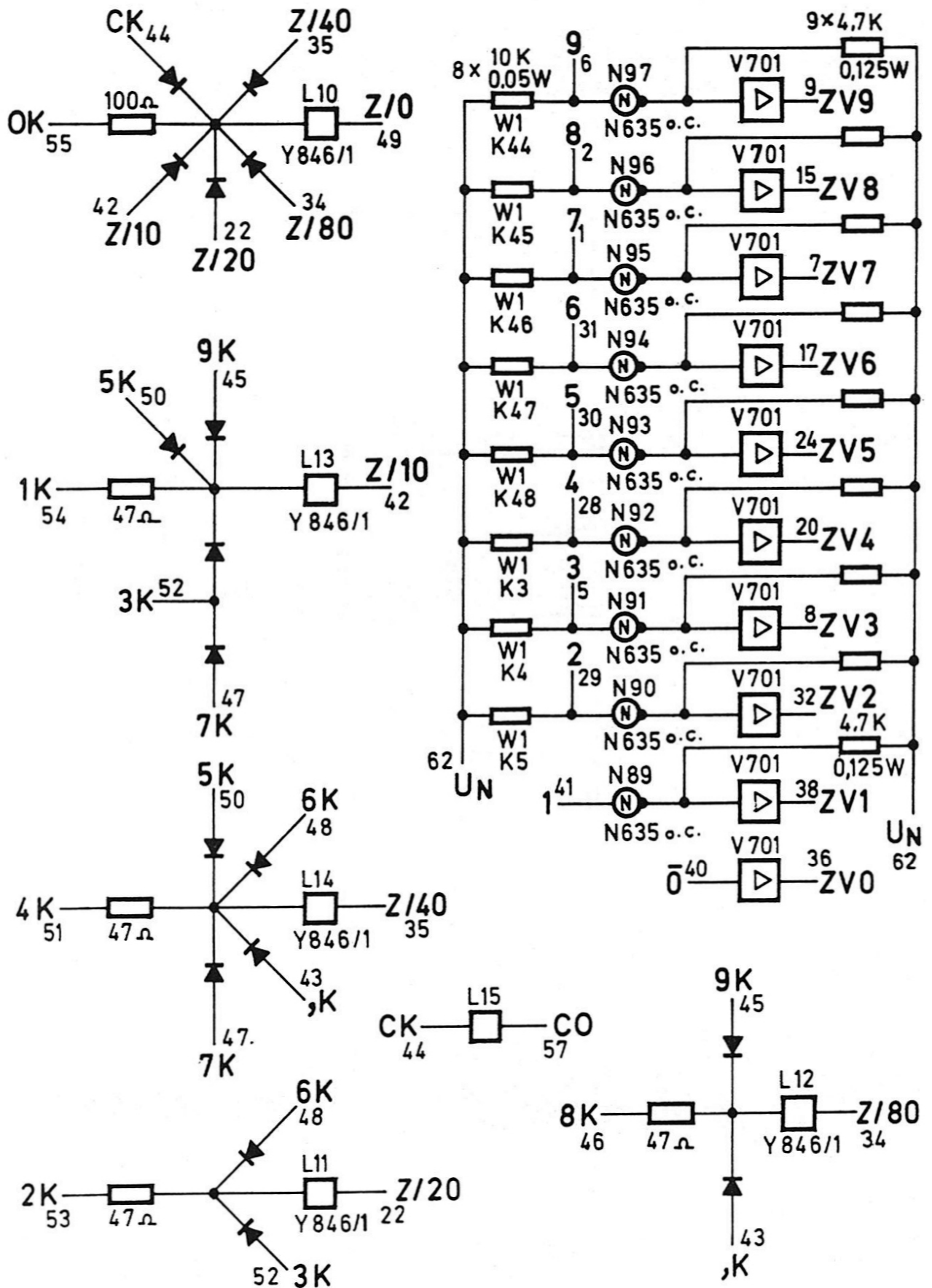
Logic diagram - Board 11



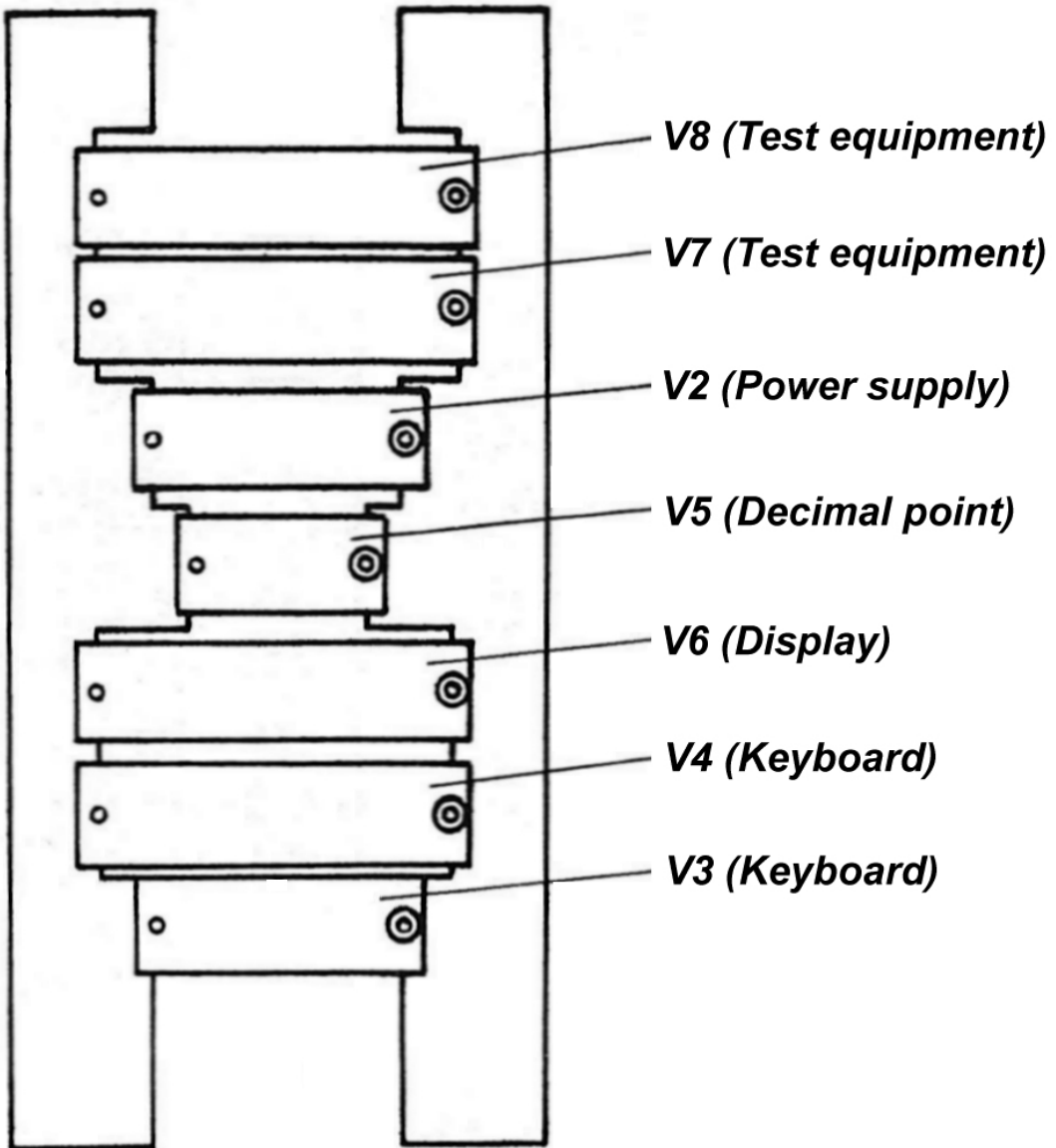
Layout plan - Board 12

1	7	1/3	
2	8	2/3	
3			
4	UA0	2/11	8V2
5	3	2/1	
6	9	5/3/4	
7	ZV7		7v6
8	ZV3		3V6
9	ZV9		9V6
10			
11	—UA		7V2
12			
13	<u>ZV9</u>		
14	<u>ZV3</u>		
15	ZV8		8V6
16	AU	2/4; 1/5	
17	ZV6		6V6
18	6		
19			
20	ZV4		4V6
21			
22	ZI20	11/4	
23			
24	ZV5		5V6
25			
26			
27			
28	4	28/1	
29	2	30/1	
30	5	30/3	
31	6	31/3	
32	ZV2		2V6
33			
34	ZI80	38/4	
35	ZI40	37/4	
36	ZV0		10V6
37			
38	ZV1	1V6	
39	Z/1o		
40	\O\	48/4; 49/9	
41	1	40/4	
42	ZI10	50/4	
43	'k		11V4
44	Ck		18V4
45	9k		9V4
46	8k		8V4
47	7k		7V4
48	6k		6V4
49	ZI0	49/8; 48/9	
50	5k		5V4
51	4k		4V4
52	3k		3V4
53	2k		2V4
54	1k		1V4
55	Ok		10V4
56			
57	CO	56/8	
58	Z/4o		
59	Z/8o		
60	OV	60/1-12	11,12V2; 5,6V3; 1V8
61	+Up	61/1-12	13V2; 21V7
62	—UN	62/1-12	14,15V2; 29V6; 20V7

Pin assignment - Board 12



Logic diagram - Board 11



Connector Layout

V7

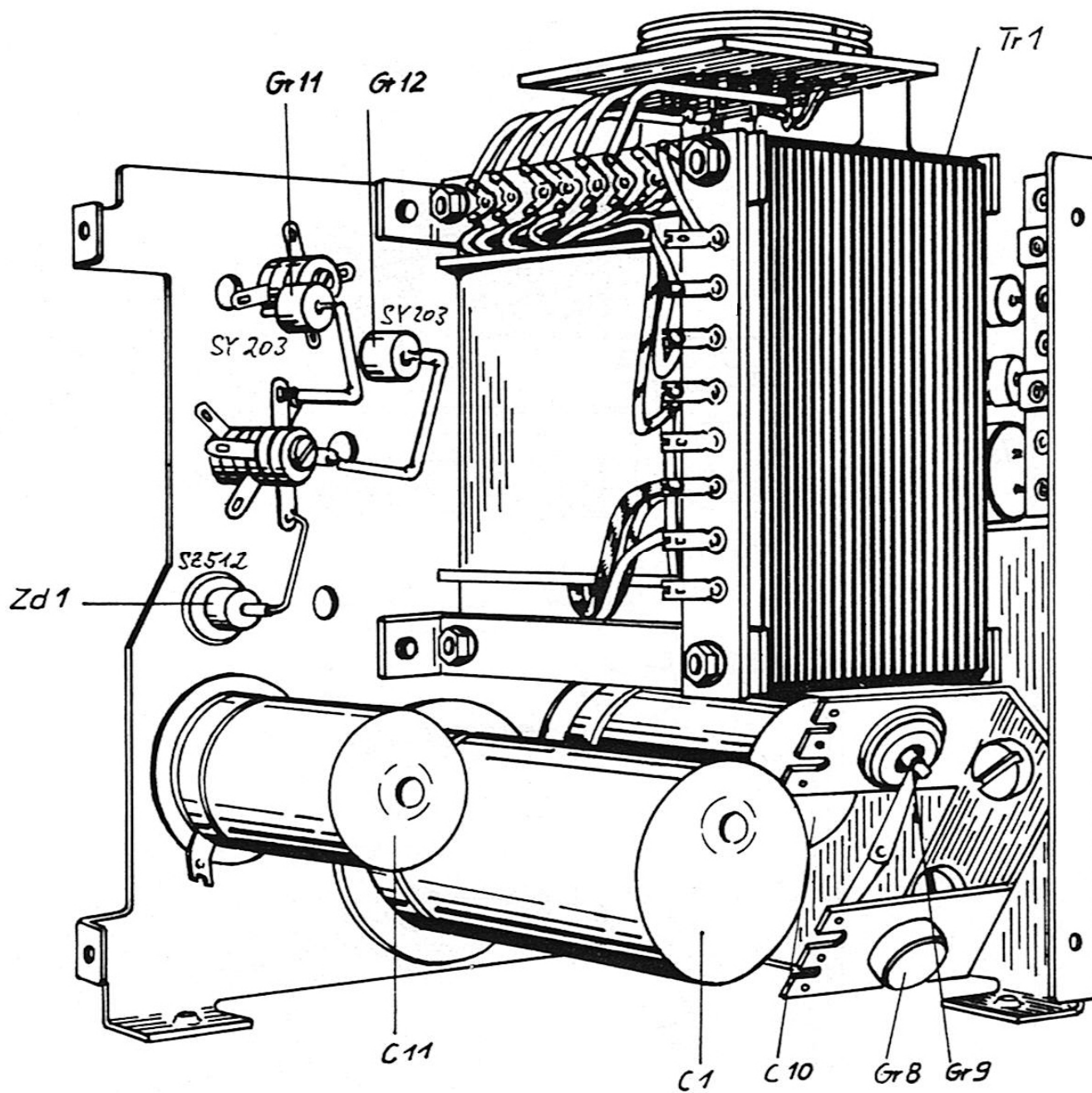
Adapter (connecting strip)			Arithmetic unit (multipole socket)	
19St1	1	E8	1	29/3
63St1	2	ÜBER	2	47/4
64St1	3	F1	3	4/5
42St1	4	F2	4	18/5
31St1	5	F3	5	8/3
2St1	6	F4	6	14/2
73St1	7	F5	7	11/2
27St1	8	F6	8	52/5
36St1	9	Z1	9	54/2
13St1	10	Z2	10	57/2
17St1	11	Z4	11	12/2
68St1	12	Z8	12	18/2
65St1	13	Z16	13	31/5
	14		14	
32St1	15	\ B1 \	15	57/3
70St1	16	B2	16	44/7
30St1	17	B3	17	46/7
28St1	18	\ B4 \	18	27/10
	19		19	
	20	-UnN	20	62/4
	21	+Up	21	61/5
	22		22	
	23	0	23	14/t1
	24	+UA	24	5V2
	25		25	
47St1	26	MV1	26	21/5
48St1	27	MV2	27	6/5
	28	AUSG	28	
	29	\ ST \	29	13/9
	30	\ ST \	30	9/2
	31		31	
	32		32	

Pin assignment V7

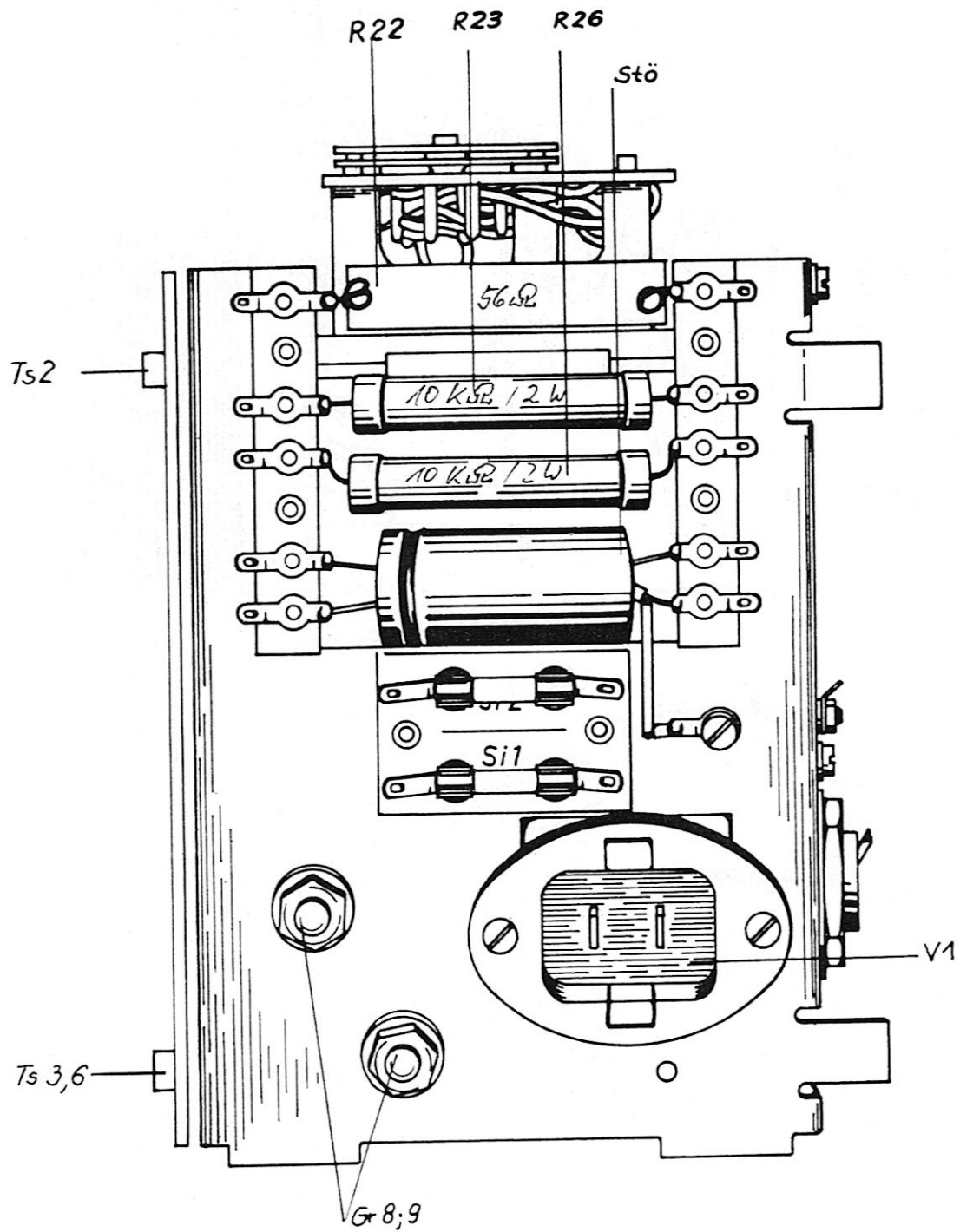
V8

Adapter (connecting strip)			Arithmetic unit (multipole socket)	
80St1	1	0V	1	60/4
7St1	2	AI	2	15/1
33St1	3	EI	3	35/3
	4		4	
14St1	5	SCHR	5	24/1
3Stl	6	M	6	9/5
5Stl	7	S1	7	36/2
	8	UV	8	
	9	AUSG	9	
	10		10	
22St1	11	MRS	11	33/2
8St1	12	A2	12	18/1
10St1	13	E2	13	21/3
	14		14	
59St1	15	V	15	37/3
	16		16	
40Stl	17	MUL	17	9/3
35St1	18	DIV	18	24/5
44St1	19	R	19	7/7
71Stl	20	HV	20	51/1
21St1	21	MDS	21	2/2
9St1	22	A4	22	44/1
16St1	23	E4	23	47/3
	24		24	
61St1	25	SUB	25	58/4
55St1	26	\ MZ \	26	9/4
41St1	27	RÜ	27	38/5
343t1	28	VER	28	40/3
45St1	29	\ VOR \	29	47/8
46St1	30	AC	30	31/2
20St1	31	ACO	31	32/2
38St1	32	A8	32	26/3

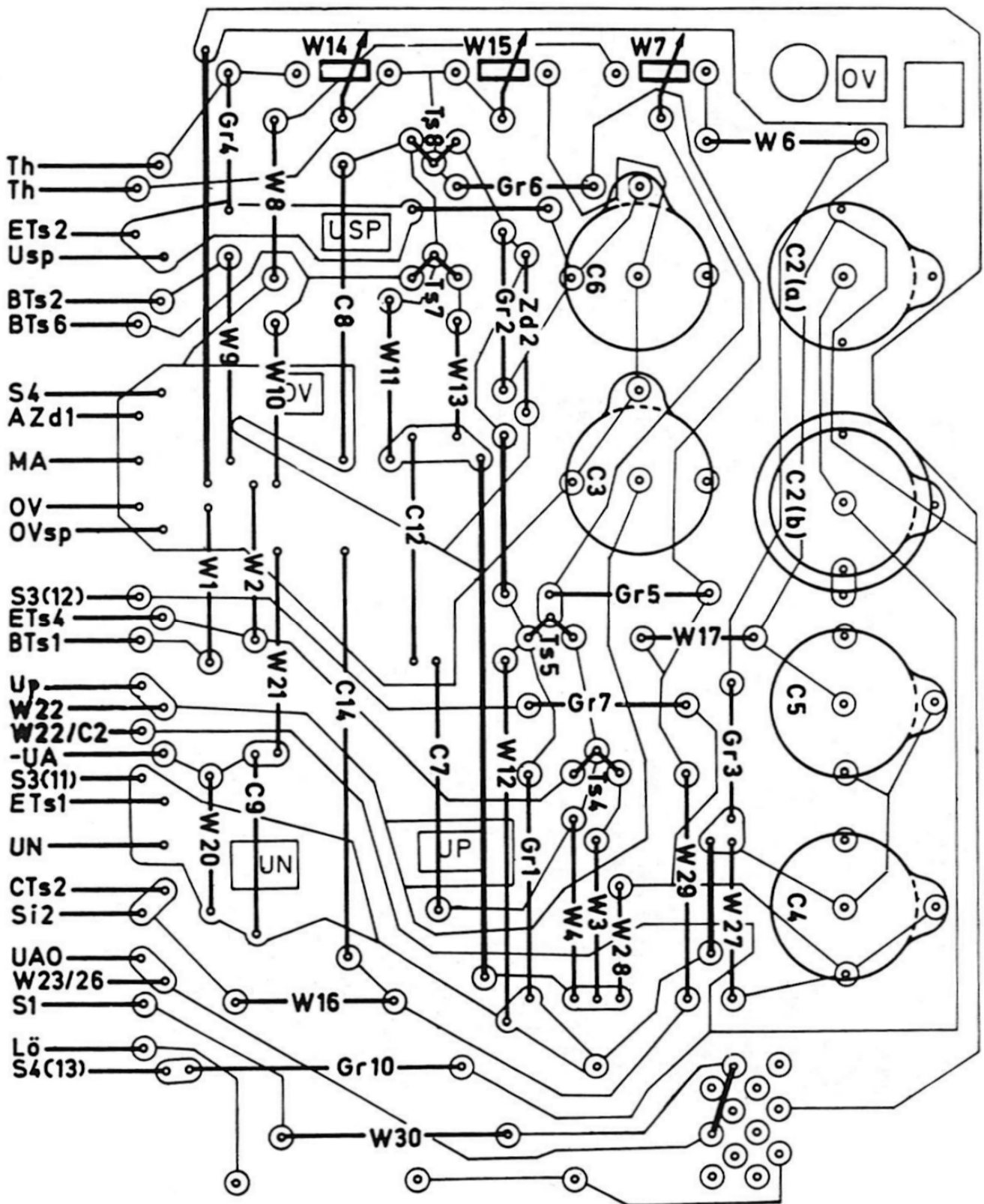
Pin assignment V8



Layout plan I - Power supply

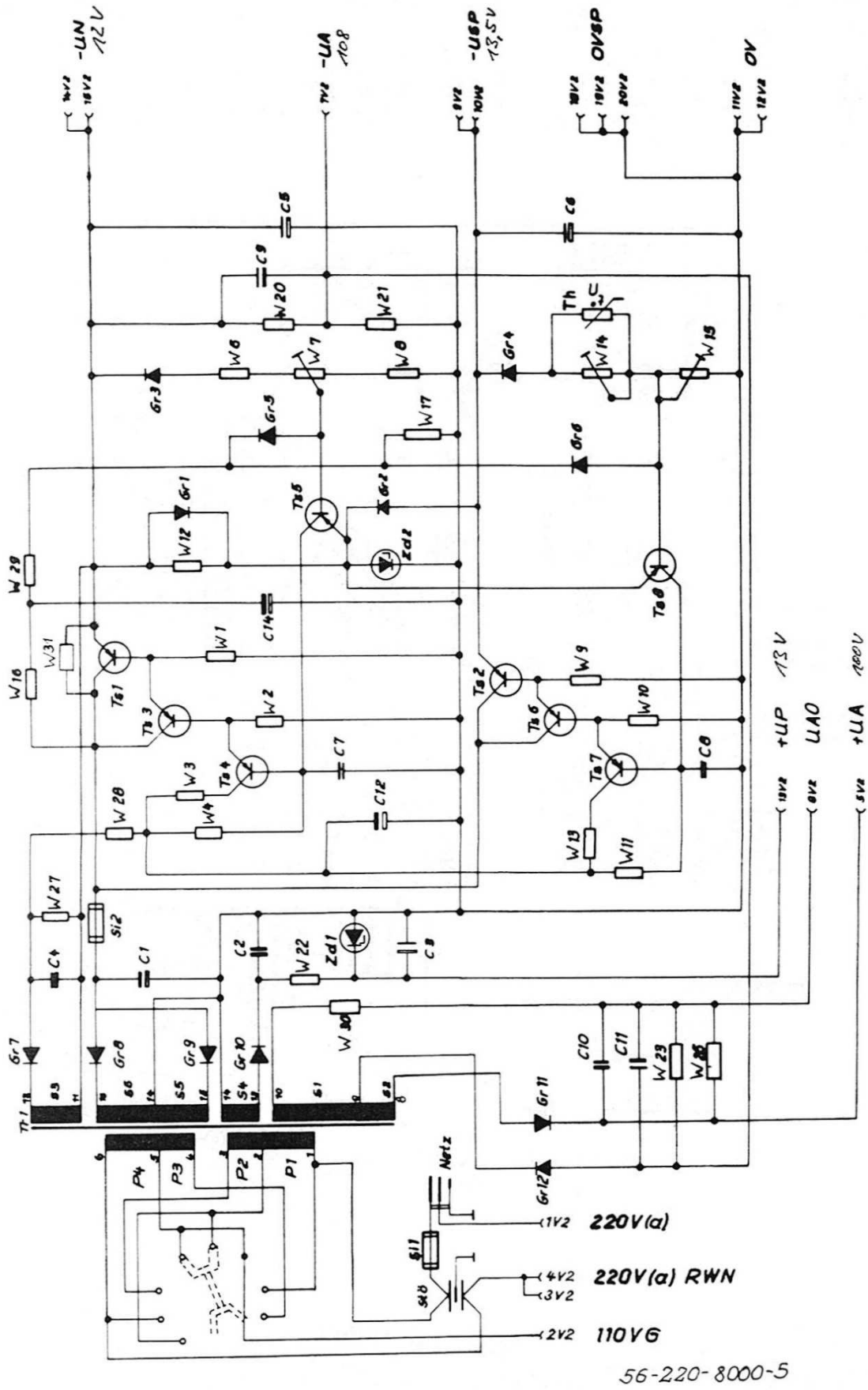


Layout plan II - Power supply



56-220-8015-0

Layout plan III - Power supply



Circuit diagram - Power supply

V1

Power supply (plug)		
1V2	1	220V(a)
Si1	2	220V(b)
Housing	3	Earth

V2

Adapter (connecting strip)			Arithmetic unit (multipole socket)	
1V1	1	220V(a)	1	3V3
5Trl	2	110VG	2	30V6
Stö	3	220V(a)RWN	3	31V6
	4	220V(a)RWN	4	1V3
Gr11; C10; R26	5	+UA	5	23V7
	6		6	
Gr12; C9,11; R20,21,23	7	-UA	7	11/12
REL1a; C10,11; R23,26	8	UA0	8	2/11
Ts2; Gr2,4; C6	9	-USp	9	20/1
	10	-Usp	10	20/1
14Trl; REL1b; Zd1,2;	11	0V	11	60/3
R1,2,8,9,10,15,17,21; OVsp	12	0V	12	60/2
Zd1; C3; R22	13	+Up	13	61/1
Ts1; 11Trl; REL1; Gr1,3;	14	-UN	14	62/1
C4,5,9; R12,20,27	15	-UN	15	62/2
REL1; REL1b	16	REL1	16	13V3
	17		17	
0V	18	0Vsp	18	14V3
	19	0Vsp	19	15V3
	20	0Vsp	20	16V3

Pin assignment V1, V2

Power supply assembly

Transistors

Ts1	SZ1015
Ts2	GD1708
Ts3	GD1708
Ts4	SA25/2
Ts5	SA25/4
Ts6	GD170B
Ts7	SA25/2
Ts8	8A25/4L

Diodes and rectifiers

Gr1	Switching diode	GAY60
Gr2	Switching diode	GA Y60
Gr3	Switching diode	GA Y61
Gr4	Switching diode	GAY61
Gr5	Germanium diode	1N35 or GAZ17
Gr6	Germanium diode	1N35 or GAZ17
Gr7	Germanium rectifier diode	GY100
Gr8	Germanium rectifier diode	GY122
or		
Gr8	Silicon rectifier diode	SY170/ 1
Gr9	Germanium rectifier diode	GY122
or		
Gr9	Silicon rectifier diode	SY171/ 1
Gr10	Germanium rectifier diode	GY112
Gr11	Silicon rectifier diode	SY203
Gr12	Silicon rectifier diode	SY203

Zener diodes

Zd1	Silicon power zener diode	SZ512
Zd2	Silicon power zener diode	SZX18/6,8

Interference suppression capacitor

Stö	Radio suppression condenser	C 0, 1+2x2500(b)220/2, 25
-----	-----------------------------	---------------------------

Germanium and Silicon diodes cannot be interchanged !

Capacitors

C1	Electrolytic capacitor	5000/25
C2	Electrolytic capacitor	1000/25
C3	Electrolytic capacitor	500/25
CL	Electrolytic capacitor	1000/25
C5	Electrolytic capacitor	1000/15
C6	Electrolytic capacitor	1000/15
C7	Paper capacitor	0,1/63
C8	Paper capacitor	0,22/63
C9	Electrolytic capacitor	5/3
O10	Electrolytic capacitor	100/150-665
C11	Electrolytic capacitor	100/150-665
O12	Electrolytic capacitor	2/50
C14	Electrolytic capacitor	20/15

Resistors

R1	Film resistor	1k2 Ω	0,25W	10%
R2	Film resistor	2,7k Ω	0,125W	10%
R3	Film resistor	390 Ω	0,05W	10%
R4	Film resistor	2,7k Ω	0,125W	10%
R6	Film resistor	560 Ω	0,125W	10%
R7	Potentiometer	1k Ω		
R8	Film resistor	1,2k Ω	0,125W	10%
R9	Film resistor	1k Ω	0,25W	10%
R10	Film resistor	5,6k Ω	0,05W	10%
R11	Film resistor	2,7k Ω	0,125W	2%
R12	Film resistor	1,2k Ω	0,125W	10%
R13	Film resistor	220 Ω	0,05W	10%
R14	Potentiometer	P 10k		
R15	Potentiometer	P 5k		
R16	Film resistor	3,3k Ω	0,125W	5%
R17	Film resistor	1,5k Ω	0,05W	5%
R20	Film resistor	200 Ω	0,05W	5%
R21	Film resistor	1k Ω	0,125W	5%
R22	Wire wound resistor	56 Ω		10%
R23	Film resistor	10k Ω	2W	10%
R26	Film resistor	10k2 Ω	2W	10%
R27	Film resistor	1k Ω	0,125W	10%
R28	Film resistor	100k Ω	0,05W	10%
R29	Film resistor	1,5k Ω	0,05W	5%
R30	Film resistor	33 Ω	0,51W	10%

Power supply adjustment and control

Proceeded in accordance with the following guidance during adjustment and/or repair of the ETR power supply:

-Un

Preparation: Adjust the mains voltage selection disk to 220V.
Connect the mains power using a variable transformer.
Connect a voltmeter between -Un and 0V.

Adjust: Set the input voltage to 220V.
Adjust -Un with R7 to 12V.

Control: With an input voltage between 187... 242V, -Un must be within the range of 11.94 to 12,06V.
Ripple voltage in all operating cases ≤ 15 mV.

-Usp

Preparation: Adjust the mains voltage selection disk to 220V.
Connect the mains power using a variable transformer.
Connect a voltmeter between -Usp and 0V.
Unsolder one side of the Thermistor, attach to the connection points of the thermistor in row two decades would resistor (0,1,2 ... 10 x 100 Ω and 0,1,2 ... 10 x 1000 Ω).

Adjust: Set the input voltage to 220V.

Set the resistance value on the decade for the thermistor value at 15°C = R(15°C).
Adjust -Usp to 13,5V with P14.

Set the resistance value on the decade for the thermistor value at 40°C = R(40°C).
Adjust -Usp to 11,5V with P15.

Switch the decade to R(15°C), -Usp must be =13,43... 13, 57V.
Case is stopped with R14 -Usp to 13,5V.

Switch the decade to, -Usp must be =11,44... 11, 56V.
Case is stopped with R15 - Usp to 11,5V.

This changing attitude

Decade = R(15°C) with R14 up -Usp=13,5V and with

Decade = R(40°C) with R15 up -Usp=11,5V taken place to itself

Decade = R(15°C) -Usp=13, 43 ... 13,57V and with

Decade = R(40°C) -Usp=11, 44 ... 11,56V without placing behind R14 and/or R15 in-regulates.

Control: Decade to R(15°C) stop.
With each input voltage between 187 ... 242V
-Usp must be =13,43 ... 13,57V.

Decade to R (40°C) stop.
With each input voltage between 187 ... 242V
-Usp must be =11,44 ... 11,56V.

Ripple voltage in all operating cases ≤ 15 mV.

Remark: Where those resistance values with 15°C and/or 40°C of thermistor to thermistor values are different, on the power supply pack there is a decal, on which are printed the values at R(15°C) and R(40°C) of the thermistor used in the power pack.

+Up

Preparation: Set the input voltage to 220V.
Connect the mains power using a variable transformer.
Connect a voltmeter between +Up and 0V.

Control: Input voltage to 187V.
+Up must be $\geq 10,8$ V.
Input voltage to 242V.
+Up must be $\leq 13,2$ V.
Ripple voltage in all operating cases ≤ 300 mV.

+Ua and -Ua

Preparation: Set the input voltage to 220V.
Connect the mains power using a variable transformer.
Connect a voltmeter between +Ua and Ua0 and/or connect between -Ua and Ua0.
Press the LÖ key to engage relay REL 1.

Control: Set the input voltage to 187V.
+Ua must be ≥ 76 V.
-Ua must be ≤ 82 V.

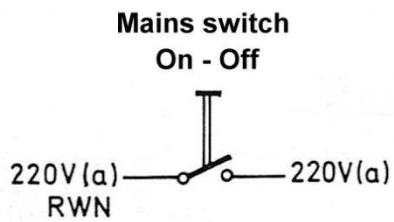
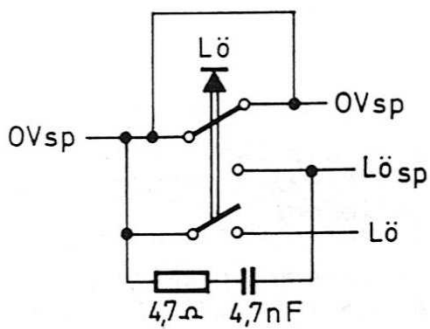
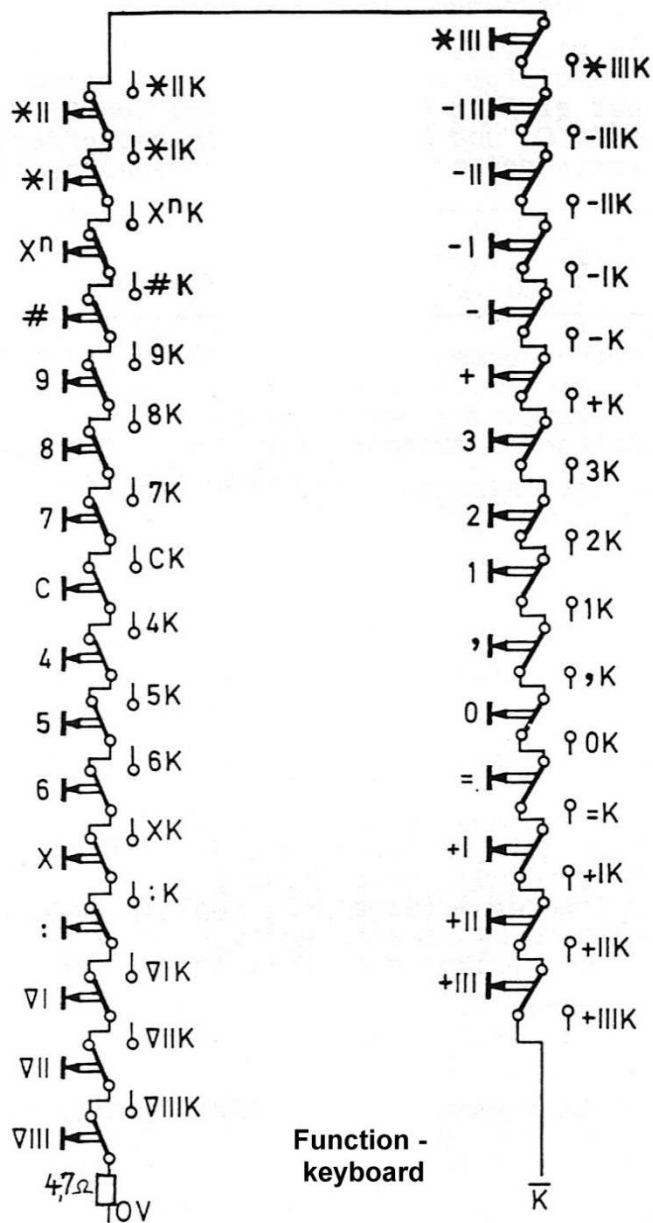
Set the input voltage to 242V.
+Ua must be ≥ 100 V.
-Ua must be ≤ 108 V.

Adjust: +Ua and -Ua are adjustable by connecting and/or changing the secondary winding S2 of the supply transformer.

110VG

Preparation: Set the input voltage to 240V.
Connect the mains power using a variable transformer.
Connect a voltmeter between 1V2 and 2V2.

Control: Set the input voltage to 240V.
The voltage between 1V2 and 2V2 must be 110V~.



Circuit diagram - Keyboard

V3

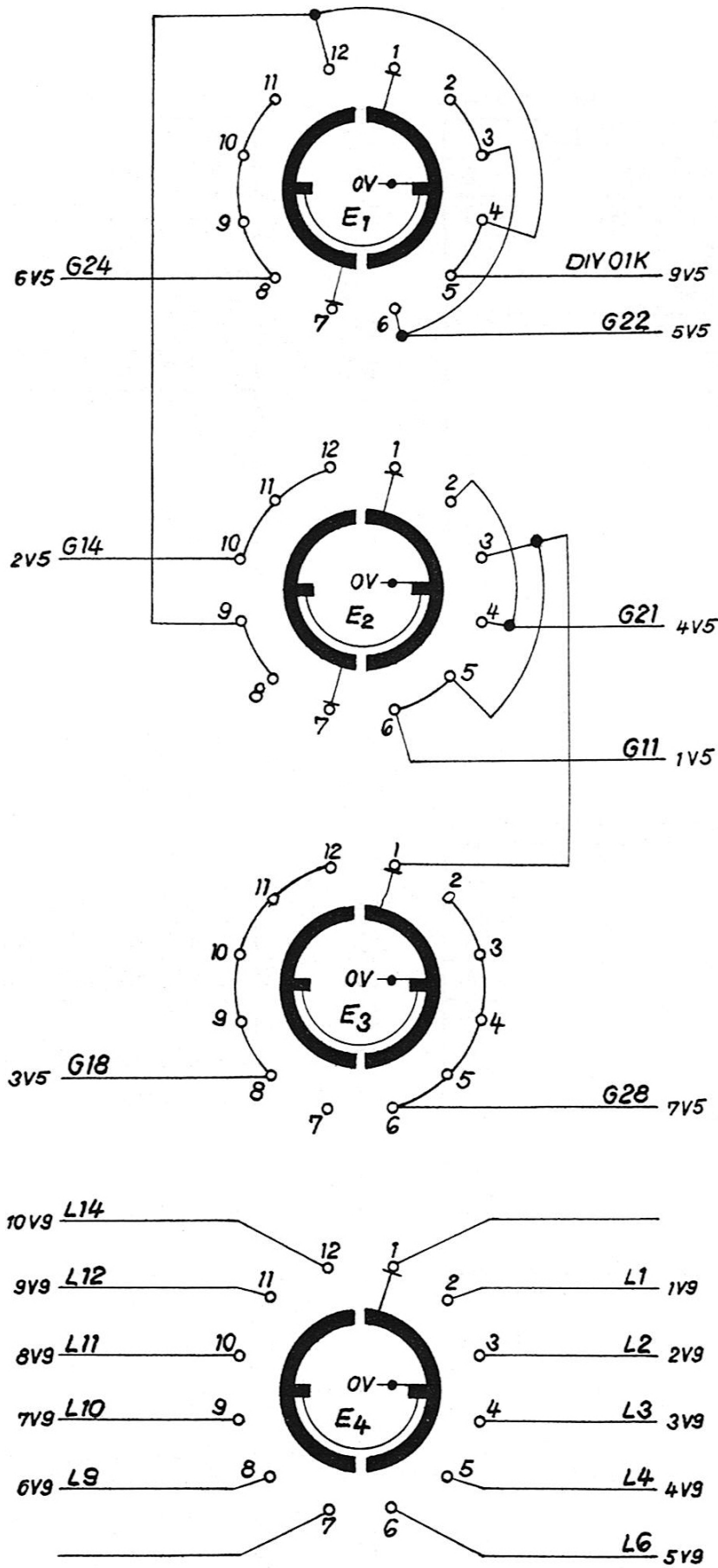
Keyboard (connecting strip)			Arithmetic unit (multipole socket)	
Change over contact "AUS-EIN"	1	220V(a)RWN	1	3V2
	2		2	
Make contact "AUS-EIN"	3	220V(a)	3	1V2
	4		4	
Change over contact "*"I"	5		5	60/1
Make contact2 "LÖ"	6		6	
Break contact "="	7	0V	7	30/9
	8	0V	8	
	9	\ K \	9	
	10		10	
	11		11	
	12		12	
Change over contact2 "LÖ"	13	REL1	13	16V2
Change over contact1,3	14	0Vsp	14	18V2
"LÖ"	15	0Vsp	15	19V2
	16	0Vsp	16	20V2
Break contact 1"LÖ"	17	0VspA	17	37/1
	18	0VspA	18	38/1
	19	0VspA	19	39/1
Make contact "#"	20	#k	20	24/11

Pin assignment V3

V4

Keyboard (connecting strip)			Arithmetic unit (multipole socket)	
Normally open contact	"1"	1k	1	54/12
Normally open contact	"2"	2k	2	53/12
Normally open contact	"3"	3k	3	52/12
Normally open contact	"4"	4k	4	51/12
Normally open contact	"5"	5k	5	50/12
Normally open contact	"6"	6k	6	48/12
Normally open contact	"7"	7k	7	47/12
Normally open contact	"8"	8k	8	46/12
Normally open contact	"9"	9k	9	45/12
Normally open contact	"0"	0k	10	55/12
Normally open contact	"+"	,k	11	43/12
Normally open contact	"+"	+k	12	22/11
Normally open contact	"-"	-k	13	21/11
Normally open contact	"x"	xk	14	41/11
Normally open contact	":"	:k	15	30/11
Normally open contact	"Xn"	xnk	16	35/11
Normally open contact	"="	=k	17	42/11
Normally open contact	"C"	Ck	18	44/12
Normally open contact	"+"	=+lk	19	27/11
Normally open contact	"+II"0	+llk	20	17/11
Normally open contact	"+III"	+lllk	21	19/11
Normally open contact	"-I"	-lk	22	33/11
Normally open contact	"-II"	-llk	23	34/11
Normally open contact	"-III"	-lllk	24	26/11
Normally open contact	"*I"	*lk	25	38/11
Normally open contact	"*II"	*llk	26	37/11
Normally open contact	"*III"	*lllk	27	25/11
Normally open contact	"vI"	vlk	28	36/11
Normally open contact	"vII"	vllk	29	40/11
Normally open contact	"vIII"	vlllk	30	31/11
Normally open contact 3	"LÖ"	Lö	31	52/7
Normally open contact 1	"LÖ"	Lösp	32	11/01

Pin assignment V4



Circuit diagram - Rotary switch

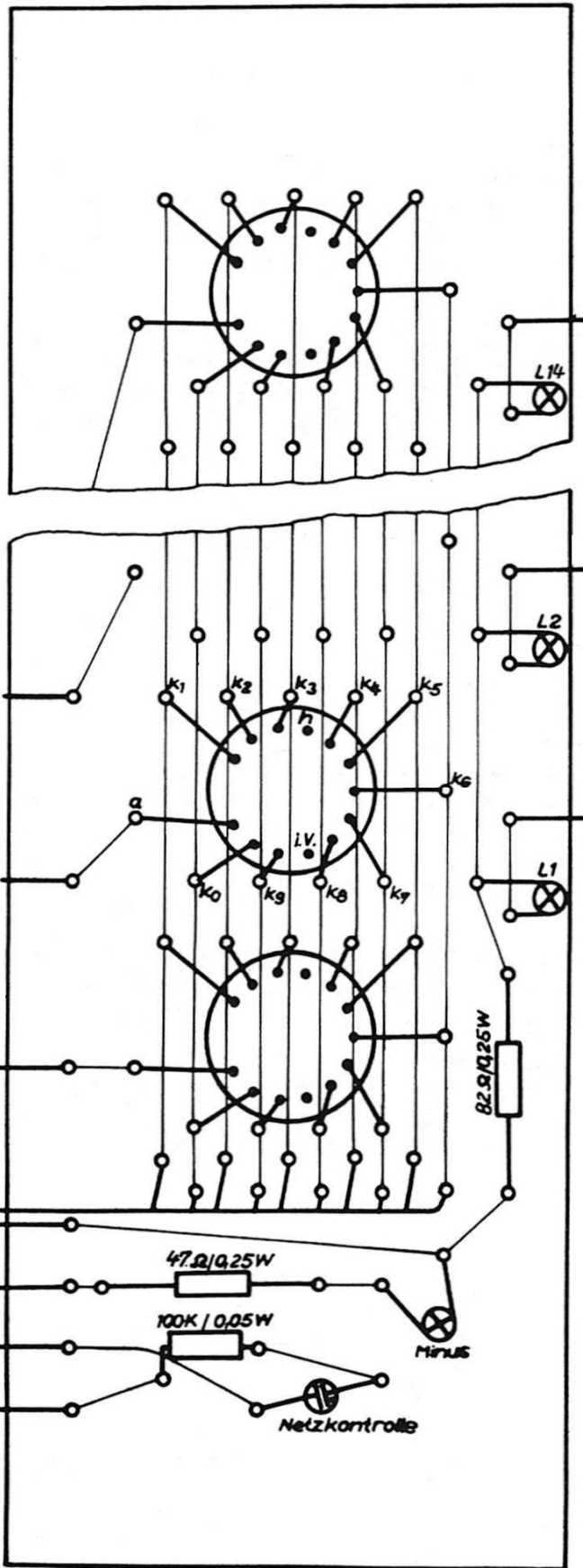
V5

Keyboard (connecting strip)			Arithmetic unit (multipole socket)	
3,5,6 level 2; 1 level 3	1	G11	1	10/10
10,11,12 level 2	2	G14	2	39/10
8,9,10,11,12 level 3	3	G18	3	18/10
2,4 level 2	4	G21	4	47/10
2,3,6 level I	5	G22	5	8/10
8,9,10,11 level I	6	G24	6	1/10
2,3,4,5,6 level 3	7	G28	7	2/10
Toggle contact from level 1,2,3,4	8	0V	8	12V2
4,5,12 level I; 9	9	DIV 01k	9	21/9
8,9 level 2	10		10	
	11		11	

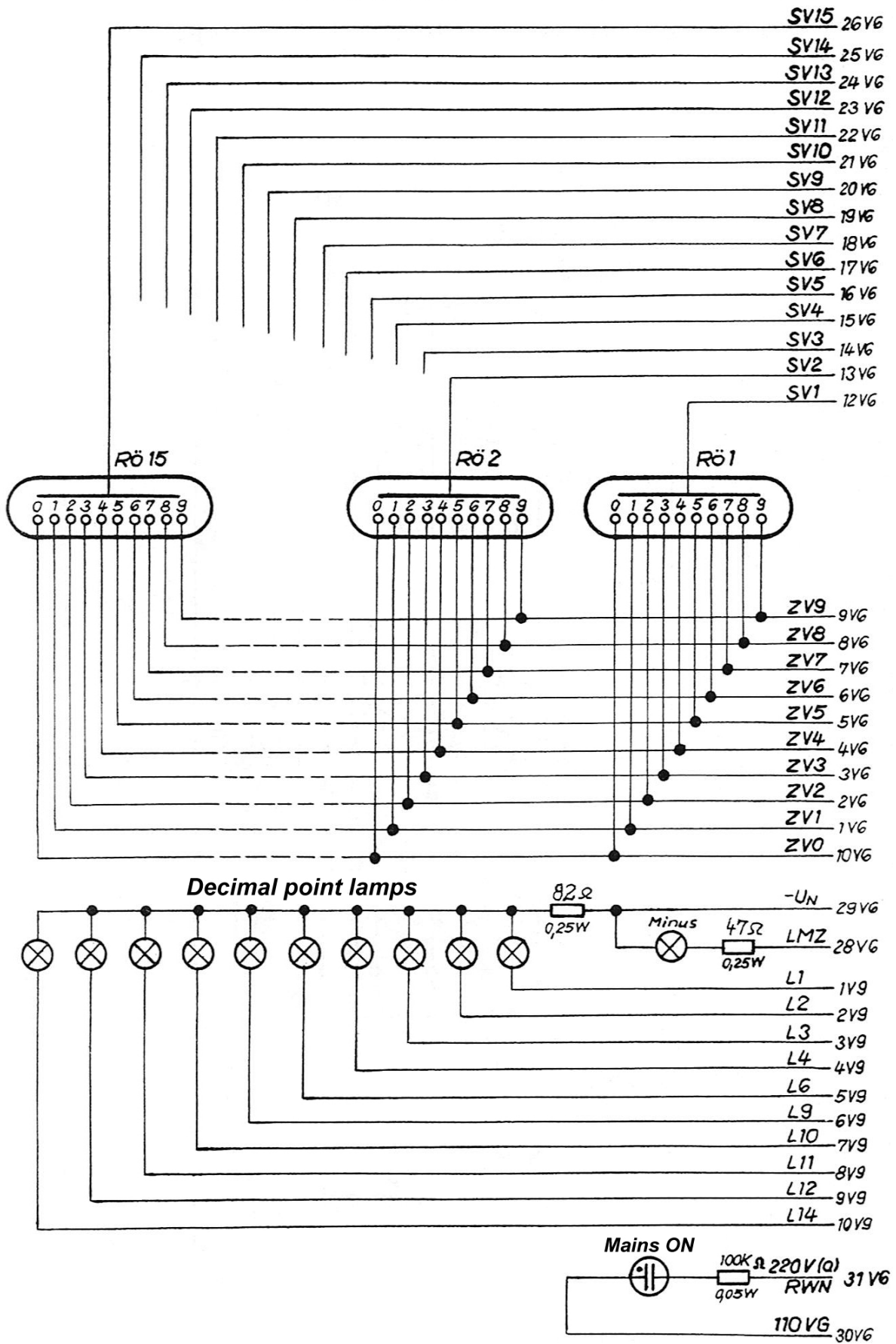
V9

Keyboard (connecting strip)			Arithmetic unit (multipole socket)	
2 level 4	1	L1	1	Decimal point lamp 1
3 level 4	2	L2	2	Decimal point lamp 2
4 level 4	3	L3	3	Decimal point lamp 3
5 level 4	4	L4	4	Decimal point lamp 4
6 level 4	5	L6	5	Decimal point lamp 6
B level 4	6	L9	6	Decimal point lamp 9
9 level 4	7	L10	7	Decimal point lamp 10
10 level 4	8	L11	8	Decimal point lamp 11
11 level 4	9	L12	9	Decimal point lamp 12
12 level 4	10	L14	10	Decimal point lamp 14
	11		11	

Pin assignment V5, V9



Layout plan - Display



Circuit diagram - Display

V6

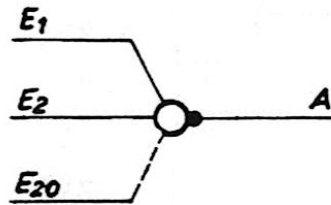
Display (connecting strip)			Arithmetic unit (multipole socket)	
Cathode 1 R \ddot{o} 1 ... 15	1	ZV1	1	38/12
Cathode 2 R \ddot{o} 1 ... 15	2	ZV2	2	32/12
Cathode 3 R \ddot{o} 1 ... 15	3	ZV3	3	8/12
Cathode 4 R \ddot{o} 1 ... 15	4	ZV4	4	20/12
Cathode 5 R \ddot{o} 1 ... 15	5	ZV5	5	24/12
Cathode 6 R \ddot{o} 1 ... 15	6	ZV6	6	17/12
Cathode 7 R \ddot{o} 1 ... 15	7	ZV7	7	7/12
Cathode 8 R \ddot{o} 1 ... 15	8	ZV8	8	15/12
Cathode 9 R \ddot{o} 1 ... 15	9	ZV9	9	9/12
Cathode 0 R \ddot{o} 1 ... 15	10	ZV0	10	36/12
	11		11	
Anode R \ddot{o} 1	12	SV1	12	4/11
Anode R \ddot{o} 2	13	SV2	13	5/11
Anode R \ddot{o} 3	14	SV3	14	6/11
Anode R \ddot{o} 4	15	SV4	15	7/11
Anode R \ddot{o} 5	16	SV5	16	8/11
Anode R \ddot{o} 6	17	SV6	17	9/11
Anode R \ddot{o} 7	18	SV7	18	10/11
Anode R \ddot{o} 8	19	SV8	19	12/11
Anode R \ddot{o} 9	20	SV9	20	13/11
Anode R \ddot{o} 10	21	SV10	21	15/11
Anode R \ddot{o} 11	22	SV11	22	16/11
Anode R \ddot{o} 12	23	SV12	23	55/11
Anode R \ddot{o} 13	24	SV13	24	56/11
Anode R \ddot{o} 14	25	SV14	25	57/11
Anode R \ddot{o} 15	26	SV15	26	58/11
	27		27	
R82 Ω /0,25W	28	LMZ	28	12/8
R270 Ω /0, 25W	29	-Un	29	62/3
Power on Lamp	30	110VG	30	2V2
R100k Ω /0,05W	31	220V(a)RWN	31	3V2
	32		32	

Pin assignment V6

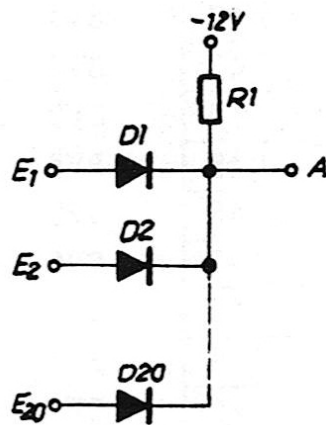
Assembly levels

Conjunction

Symbol:



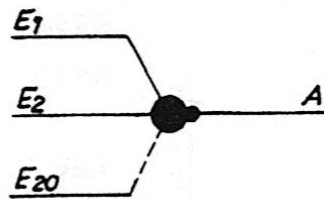
Circuit diagram:



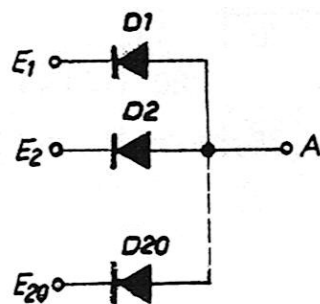
Assembly: R1 10k Ω 0,05W 10%
D1 ... D20 1N35 or GAZ17

Disjunction

Symbol:



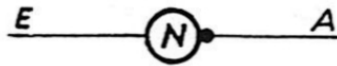
Circuit diagram:



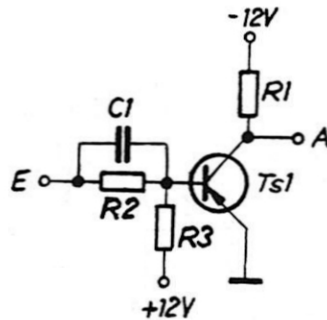
Assembly: D1 ... D20 1N35 or GAZ17

Inverter

Symbol :



Circuit diagram :

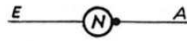


Assembly :

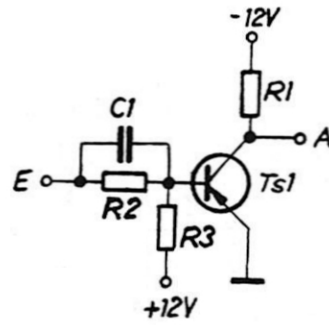
N	Ts1	C1	R1	R2	R3
630	SA25/2 $\beta=29...55$	1000/ 10/63	1,5k Ω 0,125W	12k Ω 0,05W	68k Ω 0,05W
631	SA25/3 $\beta=45...88$	1000/ 10/63	1,5k Ω 0,125W	12k Ω 0,05W	68k Ω 0,05W
632	SA25/4 $\beta=72...166$	1000/ 10/63	1,5k Ω 0,125W	12k Ω 0,05W	68k Ω 0,05W
635	SA25/4 $\beta=72... 166$	1000/ 10/63		12k Ω 0,05W	68k Ω 0,05W
636	SA25/3 $\beta=45...88$	2700/ 10/63		4,7k Ω 0,05W	39 Ω k 0,05W
637	SA25/4 $\beta=72...166$	1000/ 10/63	1,5k Ω 0,125W	4,7k Ω 0,05W	22k Ω 0,05W
649	SB20/4 $\beta=72...166$	220/ 10/63	1,5k Ω 0,125W	12k Ω 0,05W	68k Ω 0,05W
651	SB20/2 $\beta=29...55$	220/ 10/63	1k Ω 0,125W	12k Ω 0,05W	68k Ω 0,05W
652	SB20/4 $\beta=72...166$	470/ 10/63	1,5k Ω 0,125	8,2k Ω 0,05W	47k Ω 0,05W

Inverter

Symbol :



Circuit diagram :

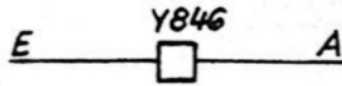


Assembly :

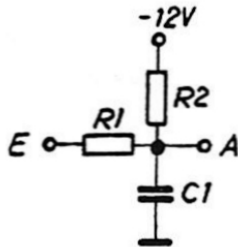
Ts1	SA25/4	$\beta=72...166$	
Ts2	SA25/4	$\beta=72...166$	
C1	1000/10/63		
C2	2200/10/63		
R1	820 Ω	0,25W	10%
R2	330 Ω	0,5W	10%
R3	2,2k Ω	0,05W	10%
R4	12k Ω	0,05W	10%
R5	69k Ω	0,05W	10%
R6	15k Ω	0,05W	10%

Line input Y846 and Y846/1

Symbol:



Circuit diagram:



Assembly:

C1	0,047/63		
R1	100Ω	0,05W	10%
R2	10kΩ	0,05W	10%

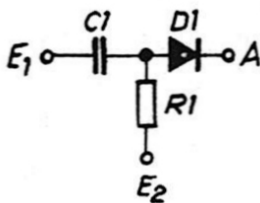
Resistor R1 is void with Y846/1.

Input

Symbol:



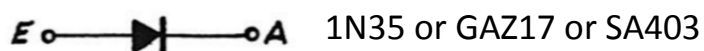
Circuit diagram:



Assembly:

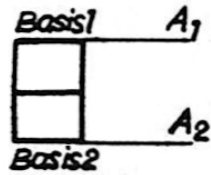
D1	SA403		
C1	560/5/63		
R1	10kΩ	0,05W	10%

Static input for F119

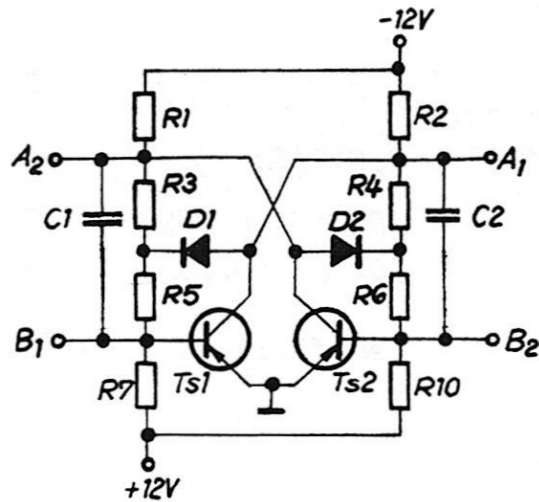


Flip—Flop F119

Symbol:



Circuit diagram:

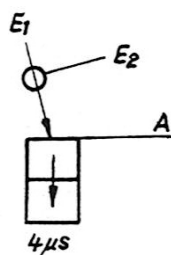


Assembly:

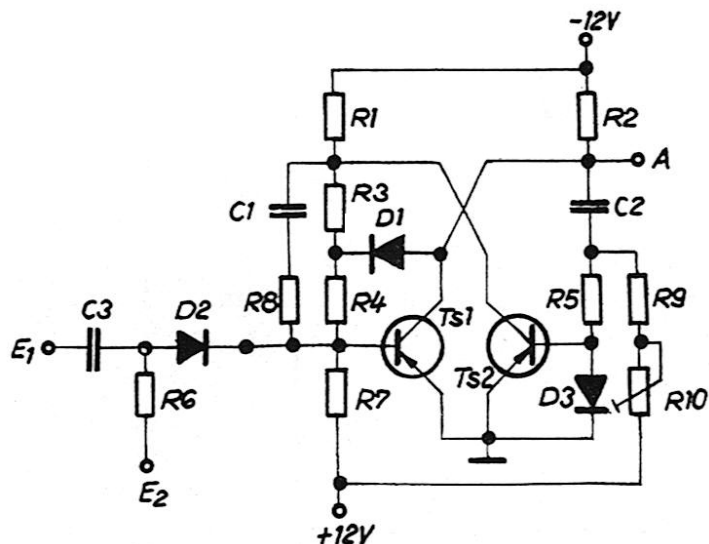
Ts1	SA25/2	$\beta=29...55/4-8\mu S$	
Ts2	SA25/2	$\beta=29...55/4-8\mu S$	
D1	1N35 or GAZ17		
D2	1N35 or GAZ17		
C1	1000/10/63		
C2	1000/10/63		
R1	1,5k Ω	0,125w	10%
R2	1,5k Ω	0,125w	10%
R3	10k Ω	0,05w	10%
R4	10k Ω	0,05w	10%
R5	470 Ω	0,05w	10%
R6	470 Ω	0,05w	10%
R7	56k Ω	0,05w	10%
R10	56k Ω	0,05w	10%

Monostable

Symbol:



Circuit diagram:

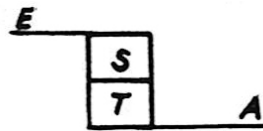


Assembly:

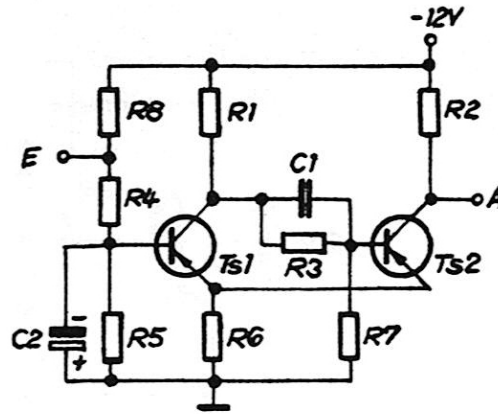
Ts1	S820/3	β 45...88	
Ts2	SB20/3	β 45...88	
O1	1N35 or GAZ17		
D2	1N35 or GAZ17	or SA403	
O3	1N35 or GAZ17	or SA403	
C1	220/5/63		
C2	680/5/63		
C3	120/5/63		
R1	1k5 Ω	0,125w	10%
R2	1k5 Ω	0,125w	10%
P3	10k Ω	0,05w	10%
R4	470 Ω	0,05w	10%
R5	1k2 Ω	0,05w	10%
R6	4,7k Ω	0,05w	10%
R7	56k Ω	0,05w	10%
R8	1k Ω	0,65w	10%
R9	4,7k Ω	0,05w	10%
R10	S 50k Ω		

Schmitt—Trigger

Symbol:



Circuit diagram:

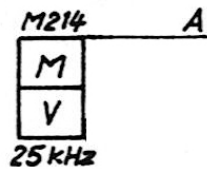


Assembly:

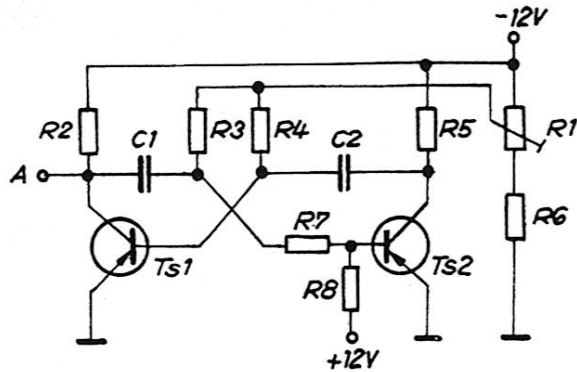
Ts1	SA25/2	$\beta=29...55$	
Ts2	SA25/2	$\beta=29...55$	
C1	2700/10/63		
C2	20/15		
R1	1,8k Ω	0,125W	10%
R2	1,5k Ω	0,125W	10%
R3	12k Ω	0,05W	10%
R4	3,9k Ω	0,05W	2%
R5	2,7k Ω	0,05w	10%
R6	82 Ω	0,05w	2%
R7	4,7k Ω	0,05w	10%
R8	2,2k Ω	0,05W	2%

Multivibrator M214

Symbol:



Circuit diagram:

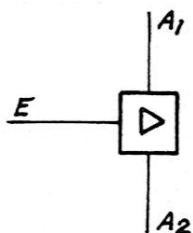


Assembly:

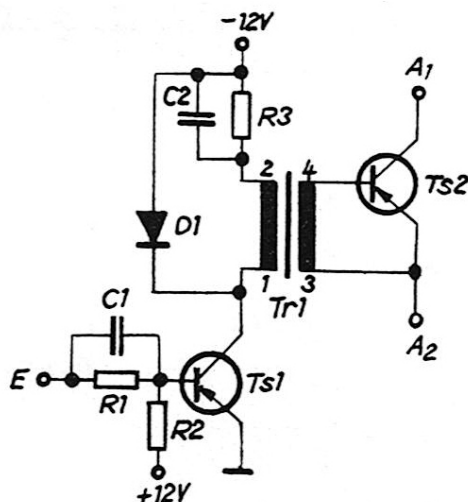
Ts1	S820/3	$\beta=45\ldots88$	
Ts2	S820/3	$\beta=45\ldots88$	
C1	2200/10/63		
C2	2200/10/63		
R1	51k	0,05w	10%
R2	1k	0,05w	10%
R3	10k	0,05w	10%
R4	10k	0,05w	10%
R5	1,5	0,125w	10%
R6	1k	0,05w	10%
R7	470k	0,05w	10%
R8	220k	0,05w	10%

Ferrite core drivers Y910, Y911 and Y912

Symbol:



Circuit diagram:

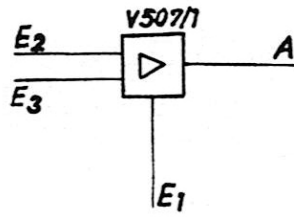


Assembly:

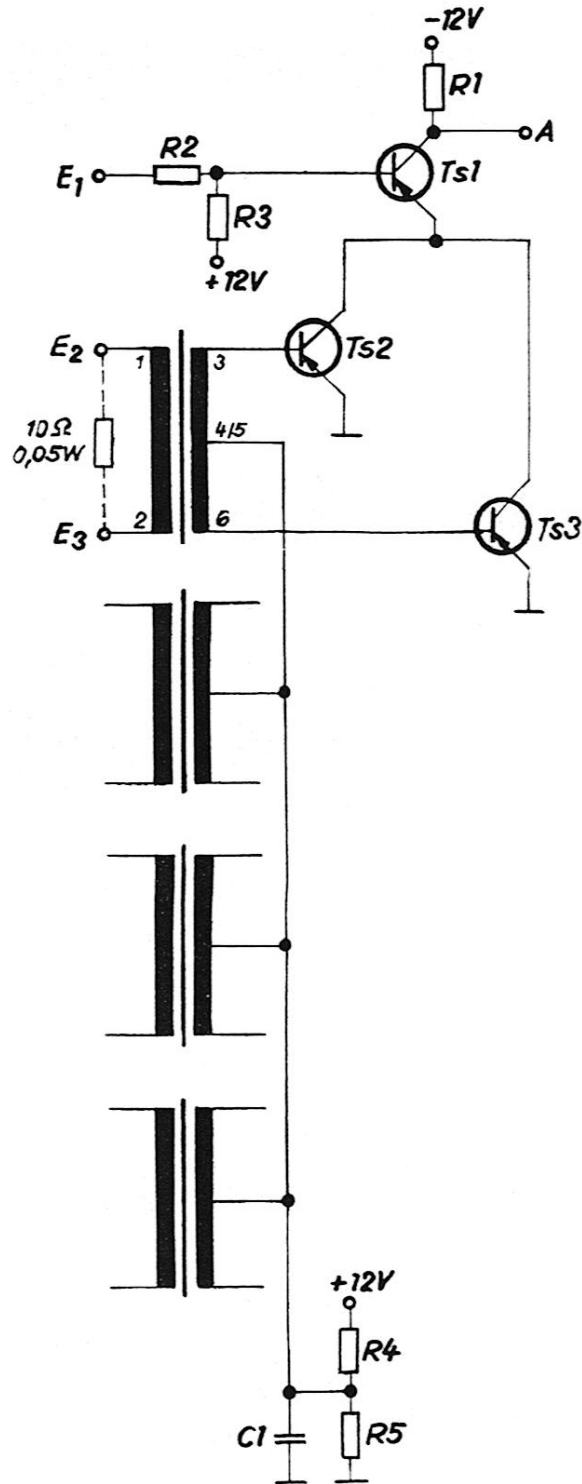
Y	910	911	912
Ts1	SB20/4 $\beta=72...166$	SB20/4 $\beta=72...166$	SB20/4 $\beta=72...166$
Ts2	SB20/4 $\beta=72...166$	SB20/4 $\beta=72...166$	SB20/4 $\beta=72...166$
D1	0A741	0A741	0A741
C1	220/10/63	220/10/63	220/10/63
C2	330/10/63	330/10/63	330/10/63
R1	12k Ω 0,05w 10%	12k Ω 0,05w 10%	12k Ω 0,05w 10%
R2	68k Ω 0,05w 10%	68k Ω 0,05w 10%	68k Ω 0,05w 10%
R3	820 Ω 0,125w 10%	820 Ω 0,125w 10%	820 Ω 0,125w 10%
Tr1	Tr 910	Tr 910	Tr 912

Read amplifiers V507/1

Symbol:



Circuit diagram:

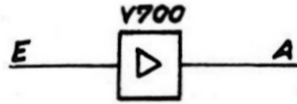


Assembly:

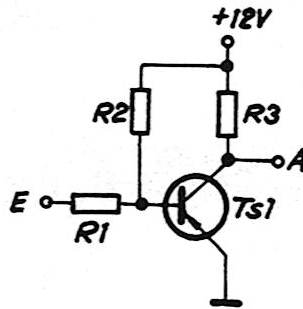
Ts1	SB20/2	$\beta=29...55$	
Ts2	SB20/3	$\beta=45...88$	
Ts3	SB20/3	$\beta=45...88$	
C1	0,047/10/53		
R1	10k Ω	0,125w	10%
P2	12k Ω	0,125w	10%
P2	68k Ω	0,125W	10%
R4	6,8k Ω	0,125w	5%
R5	100 Ω	0,125w	5%

Lamp amplifier V700

Symbol:



Circuit diagram:

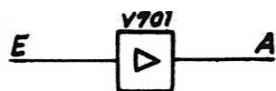


Assembly:

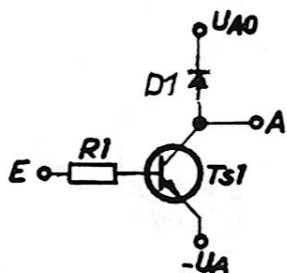
Ts1	SA25/4	$\beta=72\dots166$		
R1	10k Ω	0,05w	10%	
R2	100k Ω	0,05w	10%	
R3	1,2k Ω	0,05w	10%	

Number amplifiers (Cathodes) V701

Symbol:



Circuit diagram:



Assembly:

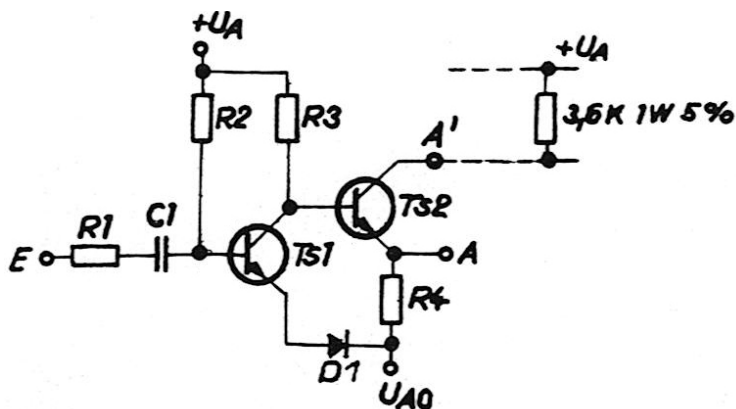
Ts1	BSY79	$\beta > 30$
R1	12k Ω	0,05w 10%
D1	KY130/150	

Place amplifiers (Anodes) V703

Symbol:



Circuit diagram:



Assembly:

Ts1	BSY	$\beta > 30$
Ts2	BSY	$\beta > 30$
C1	0,022/20/160	
R1	4,7k Ω	0,05w 10%
R2	1M Ω	0,05w 10%
R3	68k Ω	0,25w 10%
R4	100k Ω	0,125w 10%
D1	KY130/150	

Designation of the Core Memory Connections

The numbers 1. and 2. differentiate whether the connection concerned lies on the lower or on the upper plate of the magnetic core memory.

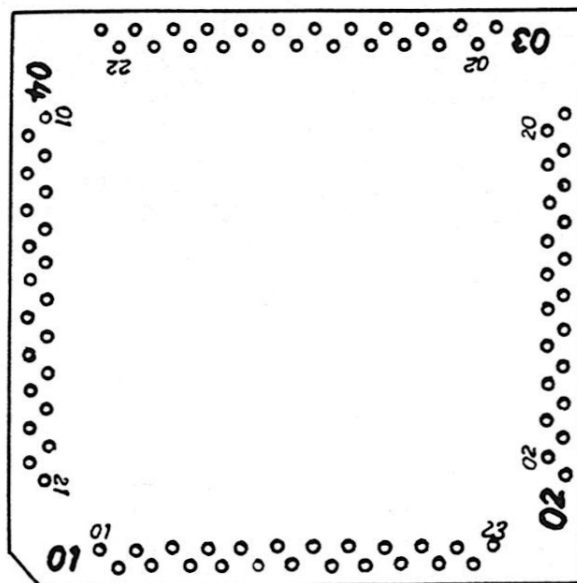
01 - lower plate

02 - upper plate

The numbers 3. and 4. differentiate which side of this plate the connection is concerned. Beginning from the tapered corner the sides are marked 03 and 04 to the right with 01, 02, one sees presupposed on the circuit paths of the plate concerned.

The numbers 5. and 6. differentiate which connection of the plate and side concerned is used. The connections of each side are listed from left to right from 01 to 23 and/or from 01 to 21 counted, again one sees presupposed on the circuit paths of the plate of the magnetic core memory.

Circuit paths



Transistor types

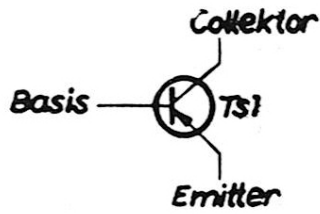
Manufacturers	Hitachi, Japan	HFO, DDR
SA25 $\beta=29...55$ Ti=4...8us 00-555-9525-6	2SB75 schwarz 00-555-9652-1	GS122 00-555-9975-8
SA25 $\beta=29...55$ 00-555-9524-8	2SB75 red 00-555-9651-3	GS121b 00-555-3307-5
SA25 $\beta=45...88$ 00-555-9526-4	2SB77 yellow 00-555-9654-6	GS121c 00-555-3308-3
SA25 $\beta=72...166$ 00-555-9527-2	2SB77 green 00-555-9655-4	GS121d 00-555-3309-1
SB20 $\beta=29...55$ 00-555-9532-8	2SA15 red 00-555-9628-7	GS109b 00-555-1106-7
SB20 $\beta=45...88$ 00-555-9533-6	2SA15 yellow 00-555-9629-8	GS109c 00-555-1107-8
SB20 $\beta=72...166$ 00-555-9534-4	2SA17 00-555-9633-7	GS109d 00-555-1108-6
SC20 $\beta=45...88$ 00-555-9544-0	2SA210 00-555-9640-0	GS111c 00-555-1128-7
SC20 $\beta=72...166$ 00-555-9547-3	2SA210 00-555-9642-5	GS111d 00-555-1129-5
1SM120	BSY79 Intermetall 00-555-9752-2	S202 only causes

Comparison list for having leader elements

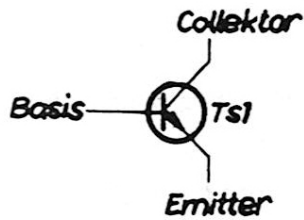
Manufacturer	Specialty		
	DDR	SW	NSW
AA2S 00-560-9520-4	GAZ17 00-560-3979-3		1N35 Hitachi 00-560-9586-6
	SY170/1 00-560-7040-5		
	SY171/1 00-560-7043-8		
	OA903 00-560-2594-8	KY130/150 00-560-9724-7	BA17/150 Telefunken 1N646 E
12ZB	SZ512 00-550-5891-7 SZ600/12		ZL512 Intermetal 00-550-5891-7
ZA 6,8	SZY18/6,8 00-560-6933-1		
	SY170/2 00-560-7041-3		
	SY171/2 00-560-7044-6		
	GS109e 00-555-1109-4		

Manufacturer	Specialty		
	DDR	SW	NSW
UE30		ASZ1015 ß=29...55 00-555-9743-4 Haungary	2SB228 Hitachi 00-555-9665-0
	GD170 00-555-0465-7		
	SY203 00-560-9639-1		
	SY200 00-550-9535-0		
	GY100 00-550-3307-2		
	GAY60 00-550-6965-2		
	GAY61 00-560-6988-7		
	GAY62 00-560-6990-1		1S79 Hitachi 00-560-9575-1
AC40 00-560-9525-3	GAY63 00-560-9600-4 OA741 00-560-2759-7	D9K SU	1S78 Hitachi 00-560-9590-3
AA25 00-560-9525-3	GAZ17 Special measurement 00-560-3981-6		1N35 Hitachi 00-560-9585-6

List circuit symbols used



PNP transistor



NPN transistor



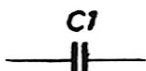
Diode



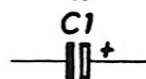
Rectifier



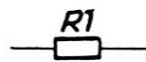
Breakdown diode



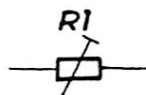
Paper or plastic film capacitor



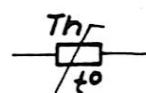
Electrolytic capacitor



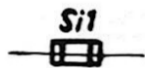
Film or wire wound resistor



Variable resistor



Thermistor



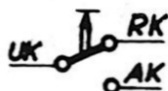
Fuse



Relay

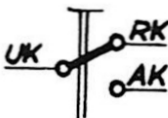


Relay contact

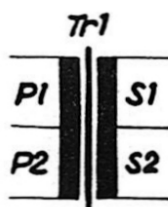


Microswitch

UK - two way contact
 RK - normally closed contact
 AK - make contact



Contact set



Transformer

P1 - Primary
 P2 - Secondary winding



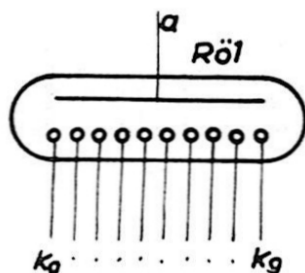
Filter capacitor



Lamp



Fluorescent lamp



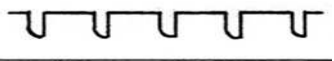
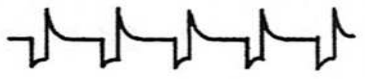
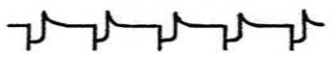
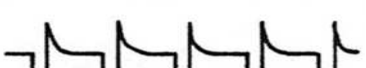

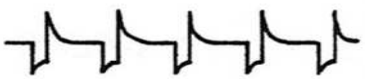

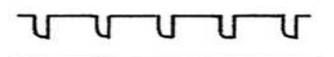

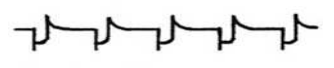

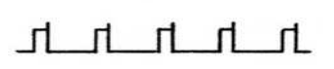
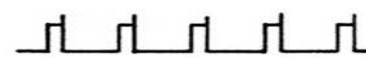

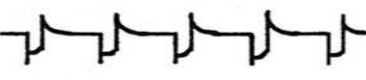
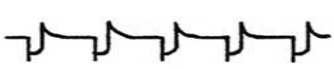
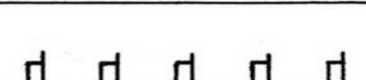
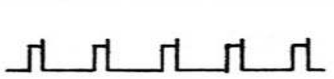
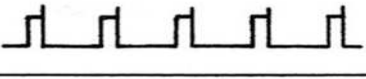
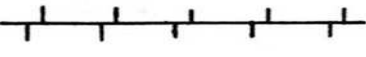
Digital indicating tube

A - Anode
 K - Cathode

Listing of transistor types

Manufacturer	Hitachi, Japan	HFO, DDR
SA25/2 β 29...55 ts=4...8uS	2SB75 black	GS121bs
SA25/2 β 29...55 ts=10uS	2SB75 red	GS121b (2)
SA25/2 β 29...55	2SB75	GS121b
SA25/3 β =45...88 ts=10uS	2SB77 gelb	GS121c (3)
SA25/4 β =72...166 ts=10uS	2SB77 green	GS121d (4)
SB20/2 β =29...55 ts=1,5uS	2SA14 red	BS109b (2)
SB20/3 β =45...88 ts=1,5uS	2SA15 yellow	GS109c (3)
SB20/4 β =72...166 ts=1,5uS	2SA17 green	GS109d (4)
SC20/2 β =29...55 ts1,2uS	2SA210 red	GS111b (2)
SC20/3 β =45...88 ts=1,2uS	2SA210 yellow	GS111c (3)
SC20/4 β =72...166 ts1,2uS	2SA210 green	GS111d (4)

Oscillograph pictures of the transistors for drivers Y910, 911, 912

Ts1 Driver Y910		TS2 Driver Y910	
Before C		At the driver	
Base		Base	
Emitter		Collector	
		Emitter	
Ts1 Driver Y911		TS2 Driver Y911	
Before C		At the driver	
Base		Base	
Emitter		Collector	
Ts1 Driver Y912		TS2 Driver Y912	
Before C		At the driver	
Base		Base	
Emitter		Collector	
		Emitter	

Ablauf über

Drücken d. Taste	Drücken d. Taste	Einsetzen der „5“	Vorzeichenverarbeitung	Ordnen der zu Komplementbildg.
B3 = L Vorzähler- durchlauf, Überführung von MR → MD, V=L MR V=L MD K107 MRS=0 D11	B3, B4 = L Vorzähler- durchlauf, keine Über- führung VOR = L R = L K141 Div = L K135	in Sp 16-K (S16=L), G2 von L → 0 über D26 Zählereinstellung auf 16-K, C1 + C4 = 0 K112 5 → ACO=L K121 MRS=0 K92 F4 = L über K171 → 5 wurde eingeschrieben	Bei U=L + Les MOS=L K105, bei V=L + Les MRS=L, bei V=L + Schr wird MRS gesperrt, U von L → 0 Abschalt- ung von A1 (VZ. MOS) durch K132 → MZ wird getriggert K157, VLS von L → 0 Abschalt- ung von A1 (VZ. MRS) → MZ wird getriggert K157, Z16 von L → 0, F3=L	0 - MD → MD, F3, F4 = L bei U=L MRS = 0 K97, bei V=L MOS = L K108, SUB = L K114, Z1 = L K185, Nach Sp. 16 schaltet F1 und F6 über K144 auf L, ADD = L, B3, B4, F1, F3, F4, F6 = L

Verschiebung	Komplement- bildung	Erster Größenvergleich und Zählung des G.V.	Letzter G.V.
F6 = 0 R.V. von MR F2, F3 = L Ein Zählerdurchlauf im Leerlauf MRS = 0 K97, VER = L und F2 = 0 über K153 → F5 = L K173 → Ordnungs- zyklus beendet, S16 von L → 0 → F1=L K144, RÜ=L K75 → R.V. von MRS, ACO=0, F2=L, VER=0, F2=0	0 - MD → MD F3, F5 = L U=L MRS=0 K97 V=L MOS=L K108 SUB=L K114 Z1 = L K185 Z16=L K194 S16 von L → 0 → F1 und F6 = L über K144 F1=L ADD=L	S 16 / ACO (MR + MD → MD) F1, F3, F5, F6 = L U=L MRS=L V=L MOS=L K104, nach G.V. F2 K169, F6=L K174 F1, F2, F3, F5, F6 = L F6=L → Zählen des G.V. A1=L K91 Z1 = 0 K185 gesperrt, da A1=L Z16=L K194 / ACO=L K120 ADD von 1 in Sp. 16 / ACO MR=0 bei U=L K83 S16 von L → 0 → F2=0 K176 keine Rückstellung / erneuter G.V.	MR + MD → MD MD > MR → F6 = L MD < MR → F6 = 0 F1, F3, F5, F6 = L U=L MRS=L, V=L MOS=L K104, nach G.V. F6 = 0 u. F2 = L, keine Zähl., F1, F2, F3, F5 = L K91 gesperrt da F6 = 0, K91 gesperrt da F6 = 0, F2=L durch F6 = 0 über K176

Ablauf der Rundung	Überführung von ACO → MR
F3, F4, F5 = L 1. Komplementbildung 0 - MD → MD F1 und F4 = L 2. G.V. die gezählt werden, Zählung wird zur Rundungsfünf welche in Sp. 16 von ACO steht dazu addiert, Nach 5. G.V. Über = L Dadurch F2 = L K176 kann nicht wirken, da Über = L, Dadurch Z1=L K181 1 + Sp. 1 / ACO über K28 ACO = L K120 Sp. 1.... Sp. 16 Weitere G.V. bis MD < MR F6 = 0 F2 bleibt L K176	<u>Löschung von ACO</u> F1, F2, F3, F4, F5 = L U = L + Les ACO=L K119 U = L + Schr. MRS=L Doppelansteuerung V = L + Les MRS=L HV=0 über K88 V = L + Schr. MRS=L Sp. 1.... Sp. 15 Sp. 16 U = L + Les ACO=L K119 HV=0 K87 U = L + Schr. MRS=L V = L + Les MRS=L HV=0 K88 V = L + Schr. MRS=L

die Division

teilenden Zahlen

Größenvergleich

$F6 = L$
 $MR + MD \rightarrow MD$
 $F1, F3, F4, F6 = L$
 bei U=L MRS
 bei V=L MOS K104
 wenn $MD > MR$ ist, ist
 $F6$ von Sp. 2 ... Sp. 16 = 0
 über K180 (VLS)
 wichtig: Nach Sp. 16
 über = 0, $\bar{0} = L$
 $MD > MR \rightarrow F6 = L$
 $F2 = L$ K 169

B3, B4, F1, F2, F3, F4 = L

Größenvergleich

$F6 = 0$
 $MR + MD \rightarrow MD$
 Wenn $MD < MR$ ist, ist
 $F6$ von Sp. 2 ... Sp. 16 = 0
 über K180 (VLS)
 In Sp. 16 über = L
 Dadurch bleibt $F6$
 auf 0 K174
 $F2 = L$ über K169

Ordnen der zu teilenden Zahlen

Rückstellung

$MR + MD \rightarrow MD$
 $F1, F2, F3, F4 = L (F6 = L)$
 $SUB = L$ K115 (da $F2 = L$)
 $Z1 = L$ K185
 SUB von Sp. 1 ... Sp. 15
 $U = L$ MRS
 $V = L$ MOS K108
 nach Sp. 16 wird $F1 = 0$
 $K149 \rightarrow VER = L$

Verschiebung

$F6 = L$
 L.V. von MR und R.V. von ACO
 $F2, F3, F4, F6 = L$
 VER von L $\rightarrow 0 \rightarrow Z1 = L$
 $K185$,
 $F2 = 0$, $VER = L$ über K153,
 L.V. von MR,
 $F1 = L$ K144,
 $RÜ = L$ K75,
 $ACO = L$ K122,
 Beachte: Aufzeichnungen

Rückstellung

$MR + MD \rightarrow MD$
 $F1, F2, F3, F5 = L$
 $SUB = L$ K113
 $U = L$ MRS = L
 $V = L$ MOS = L K108
 $S16$ von L $\rightarrow 0$ $F1 = 0$ K149
 Wenn Z1 und Z16 einschaltet
 geht VER auf L K155,
 $F6 = 0$

Linksverschiebung von MD,
 $F5 = 0$, $RÜ = 0$,
 $F2, F3, F5 = L$
 $MD = L$ K106
 $Z1 = L$ K185
 $F2 = 0$ K153
 $VER = L$
 $F1 = L$ K144
 $ACO = L$

Verschiebungen von MD u. ACO

Linksverschiebung von ACO,
 $F1, F2, F3, F5 = L$
 $ACO = L$ K122,
 $Z1, F2 = L$ K169,
 $VER = L$,
 VER G.V. von Sp. 16 / ACO nach
 Sp. 1 / ACO,
 Wenn die „5“ von Sp. 15 / ACO
 nach Sp. 16 / ACO gelangt, geht
 $F4$ auf L K170,
 $VER = 0$ K159, $F2 = 0$ K177
 $F1 = 0$ K149,

Ende der Div und VZ.-Bildung

Sp. 16 von L $\rightarrow 0$ B3 = 0 K133, B4 = 0 K134
 B3 von L $\rightarrow 0 \rightarrow Div = 0$, R = 0 K142
 Div von L $\rightarrow 0 \rightarrow F2 = 0$
 R von L $\rightarrow 0 \rightarrow F1 = 0$
 $F3 = 0$
 $F4 = 0$
 $F5 = 0$
 G2 Schaltflanke von L $\rightarrow 0$
 \rightarrow Zählereinstellung auf 16 - k
 Sp. 16 von L $\rightarrow 0 \rightarrow C1 = 0$ über K152
 $VZ = L$ (- in MR)

Ergänzungen: